

Electrical Characteristics of NO Nitrided SiO_2 Grown on p-type 4H-SiC

H. F. Li, S. Dimitrijević, H. B. Harrison, D. Sweatman, and P. Tanner

Abstract—This paper presents the results of NO nitridation of SiO_2 grown on p-type 4H-SiC. NO nitridation has a beneficial effect on the quality of the oxides grown on p-type 4H-SiC. The C-V curves become smoother and sharper after NO annealing. Frequently observed interface ledge is also removed from NO annealed samples.

I. INTRODUCTION

SiC has recently attracted a lot of attention due to its excellent material properties which promise high temperature, high power, and high frequency applications. Because of the great success of MOSFET-based electronics in silicon and the fact that thermal silicon dioxide can be grown on SiC in the same way as silicon, it is desirable to implement high-performance MOSFETs in SiC. Obtaining high quality of SiO_2 grown on SiC is a key technology to reach these aims. Previous research results indicated that the quality of the SiO_2 thermally grown on n-type SiC is comparable to oxides thermally grown on Si, but oxides thermally grown on p-type SiC exhibited poorer characteristics. Researchers have investigated the effect of post-annealing in argon[1], wafer load and withdraw procedure[2], and reoxidation[3] on the interface characteristics of SiO_2/SiC . These methods proved to be effective in improving the interface characteristics of SiO_2/SiC . We have investigated the effect of nitridation in NO and N_2O on the interface characteristics of SiO_2 on 6H-SiC[4], [5]. NO annealed samples showed improved interface of $\text{SiO}_2/\text{n-type 6H-SiC}$ while N_2O annealing adversely affect the interface characteristics. In this paper we present the results of NO annealed interface characteristics of oxides grown on p-type 4H-SiC.

II. EXPERIMENTAL DETAILS

The aluminum doped p-type 4H-SiC wafer used in this paper had a doping concentration of $3.4 \times 10^{18} \text{cm}^{-3}$ which is commercially available from CREE Research, Durham, NC, USA. The wafer was cleaned in a mixture of H_2SO_4 and H_2O_2 followed by a standard RCA cleaning procedure. Between the cleaning steps, the wafers were kept in running DI water. Immediately before the

oxidation, the wafer was dipped in 1% HF for 60 s. The wafer was oxidized in quartz furnace at 1150°C for 1.5 h. After the oxidation, the wafer was cut and one set of samples was annealed in NO in an AG610 rapid thermal processing (RTP) unit. The NO annealing was performed in three 5-min steps (to allow cooling of the RTP unit) at about 1100°C . After the oxidation and annealing, aluminum was evaporated on the top of the samples. MOS capacitors were formed by defining the circular dots by photolithography process. Aluminum was also evaporated on the back of the sample to make a large contact.

III. RESULTS AND DISCUSSION

Electrical measurements were performed using a computer-controlled HP4284 LCR meter. The p-type 4H-SiC MOS capacitors were characterized by the high-frequency capacitance (C-V) curves which were measured in dark and with UV illumination. Fig. 1 shows the typical high-frequency C-V curves for the as-grown and NO annealed samples measured in dark. The sweep rate was 0.1V/s for all measurements. The

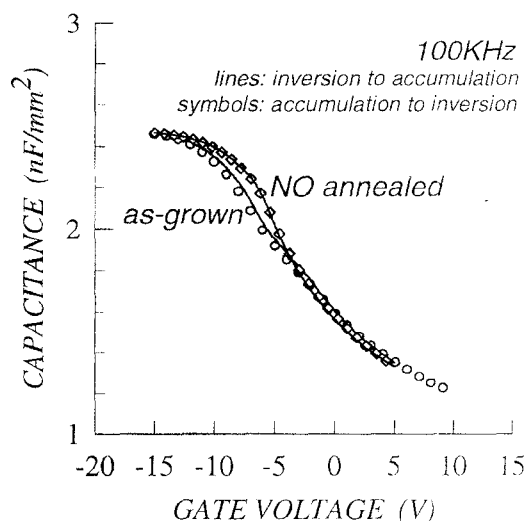


Fig. 1. High frequency C-V characteristics of the as-grown and NO annealed p-type 4H-SiC MOS capacitors measured in dark.

voltage sweep was performed in both directions (accumulation to inversion and inversion to accumulation) as

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shown in the figure. The as-grown sample shows poorer C-V characteristics, while *NO* annealing improves the C-V characteristics. Compared to the C-V curves of the as-grown sample, the C-V curves of the *NO* annealed sample are shifted positively, and are smoother and sharper. A hysteresis is also observed in the C-V curves of the as-grown sample for the two sweeping directions. *NO* annealed sample shows little hysteresis. These results indicate that good quality oxides with less net oxide charge and lower interface trap density can be obtained by *NO* annealing. The flat band voltages of the as-grown and *NO* annealed samples are $-10.10V$ and $-8.66V$, respectively. The fixed positive oxide charge Q_f of the as-grown and *NO* annealed samples calculated from the flat band shift are $11.45 \times 10^{12} cm^{-2}$ and $9.27 \times 10^{12} cm^{-2}$, respectively. To examine the interface characteristics throughfully, high frequency C-V measurements were performed under UV illumination which are shown in Fig. 2 and Fig. 3 for the as-grown sample and *NO* annealed sample, respectively. The

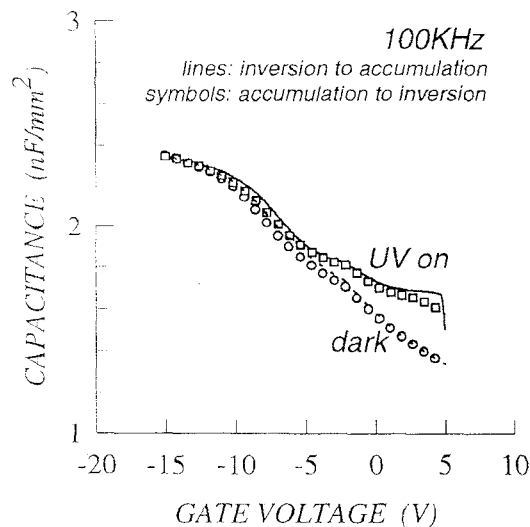


Fig. 2. High-frequency C-V characteristics of the as-grown p-type 4H-SiC MOS capacitors measured in dark and with UV illumination.

as-grown sample shows a large shift between C-V curves measured in the dark and under UV illumination. This shift is believed to be due to filling of interface traps[6]. The *NO* annealed sample shows slight shift between C-V curves measured in dark and under UV illumination which indicates an improvement in $SiO_2/4H-SiC$ interface.

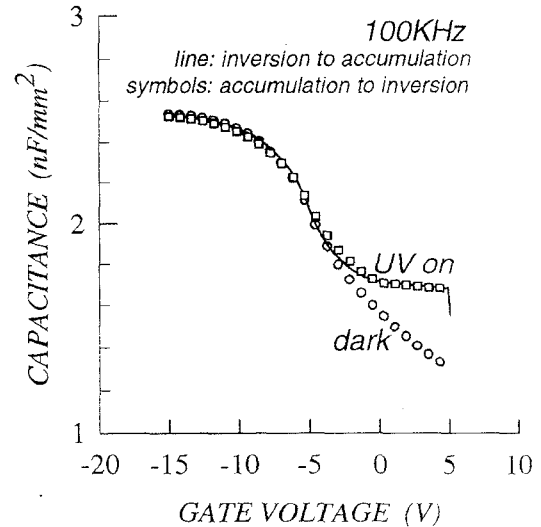


Fig. 3. High frequency C-V characteristics of the *NO* annealed p-type 4H-SiC MOS capacitors measured in dark and with UV illumination.

IV. CONCLUSIONS

The electrical characteristics of *NO* annealed oxides grown on p-type 4H-SiC have been investigated. The results show that the quality of the oxides thermally grown on p-type 4H-SiC can be improved by annealing in *NO* environment.

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