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Modeling of Integrated Circuit Yield Loss Mechanisms

Z. Stamenković, N. Stojadinović, and S. Dimitrijev

Abstract— **A yield model suited for application in a yield control system and based on in-line inspections of control wafers containing the corresponding test structures has been proposed. It is shown that the proposed yield model and yield control system can be used for modeling yield loss mechanisms and predicting efficient investments which are required in order to ensure a competitive yield of integrated circuits. An approach for the extraction of chip critical areas associated with the corresponding yield loss mechanism has been described.**

I. Introduction

A yield model which does not require any defect or fault density determination but is completely based on the test structure yield measurement and is suited for the integrated circuit production control has recently been proposed [2]. It will be shown that the above-mentioned yield model not only can be used for a successful integrated circuit production control but offers a sophisticated characterization of the integrated circuit yield loss mechanisms. In particular, after a brief description of the model itself, it will be shown how the characterization of yield loss mechanisms can be used to properly design investments in the integrated circuit production process.

II. Yield Loss Mechanism Characterization

A. Yield Parameters

Using corresponding in-line measurements of the test chip yield which will be denoted by Y_{ti} and defined as the ratio between the number of good test chips and the total number of test chips in a given wafer area, the integrated circuit chip yield, associated with the ith critical process step, can be directly predicted. The integrated circuit chip yield will differ from the test chip yield due to the difference in so-called active or critical area [1]. So, if the ratio between the integrated circuit chip and test chip critical areas is given by A_{ci}/A_{ti}, and the wafer area can be divided into m subareas with approximately uniform distribution of faults, the integrated circuit chip yield can be determined by [2], [3]

$$Y_{cil} = Y_{til}^{A_{ci}/A_{ti}} \tag{1}$$

where l denotes the corresponding subarea. However, the chip yield is not enough for complete yield characterization, and the wafer yield Y_i, defined as the ratio between the number of good chips n and the total number of chips in a wafer N, should be predicted as well. It is important to note that the number of good chips in a wafer and the wafer yield are stochastic variables, and they appear through their distribution functions [2]. The parameters of the wafer yield distribution function, the mean $\bar{Y}_i$ and the variance $\sigma^2_{Y_i}$, are given by [2]

$$\bar{Y}_i = \sum_{l=1}^{m} C_{il} Y_{cil} \tag{2}$$

$$\sigma^2_{Y_i} = (1/N) \sum_{l=1}^{m} C_{il} Y_{cil}(1 - Y_{cil}) \tag{3}$$

where C_{il} is equal to the l-th subarea divided by the total wafer area. The values of these parameters can now be used to decide about possible corrective action. If the control wafer area has been divided in the same way for each critical process step ($C_{il} = C_l$) the final chip yield is given by

$$Y_{cl} = \prod_{i=1}^{k} Y_{cil}, \quad \text{for } (l = 1, \ldots, m) \tag{4}$$

where k is the total number of critical process steps, i.e., the total number of yield loss mechanisms. At the end, the final wafer yield should be modeled as well. It has been shown that the parameters of the final wafer yield distribution (the mean $\bar{Y}$ and the variance σ^2_Y) can be approximated by [2]

$$\bar{Y} = \sum_{l=1}^{m} C_l Y_{cl} \tag{5}$$

$$\sigma^2_Y = (1/N) \sum_{l=1}^{m} C_l Y_{cl}(1 - Y_{cl}). \tag{6}$$

When the production of integrated circuit wafers is completed, a comparison between the final wafer electrical test results and the projected final wafer yield should be made in order to verify the yield control procedure. Namely, if there is significant discrepancy between the projected yield and the test results, it would be an indication that in-line inspections are not properly conceived or/and some yield loss mechanisms are missed, and corrections should be done.

B. Extraction of the Critical Area

Yield models generally require the estimation of chip critical area associated with each type of catastrophic defects, i.e., each type of primitive failures. Two most significant types of primitive failures in integrated circuits related to layer structure of integrated circuit are a vertical short of two horizontal conducting layers through oxide caused by a pinhole and a leakage current increase due to defects of silicon crystal lattice in the depletion region of p-n junction. The critical area for both of them can be defined as an overlap area of layout patterns from different integrated circuit conducting layers (silicon, polysilicon, or metal), i.e., integrated circuit mask layers [7]. Consider an example shown in Fig. 1, where two layout patterns from two different mask layers are overlapping. If $(x1, y1)$ and $(x2, y2)$ denote *canonical coordinates of overlap area*, then the overlap area A_p is given by

$$A_p = (x2 - x1) \cdot (y2 - y1). \tag{7}$$

On the other hand, two most significant types of primitive faults in integrated circuits related to very small critical dimensions of integrated circuit layout patterns are short and open circuits caused by

Manuscript received March 28, 1994; revised October 7, 1995.

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Publisher Item Identifier S 0894-6507(96)03268-X.

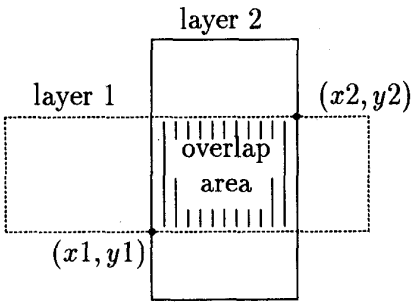

Fig. 1. The definition of critical area of vertical short as an overlap area of two geometrical objects from two different integrated circuit mask layers.

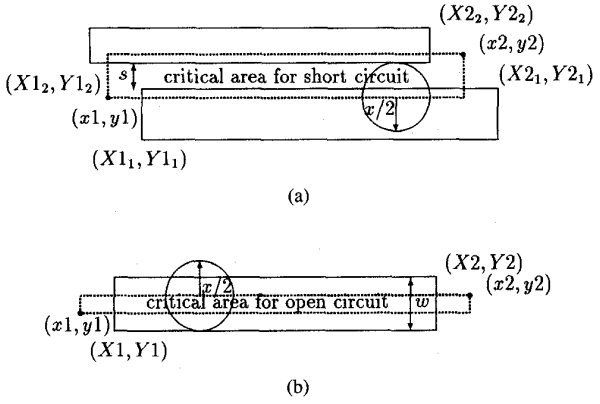

Fig. 2. The definition of *equivalent critical areas* for (a) short and (b) open circuits between geometrical objects from the same integrated circuit mask layer.

lithographic defects. The critical area for both of them can be defined as an area in which the center of a defect must fall to cause one of these faults. If the assumption of circular defects is valid, the critical area is a function of the defect diameter x. Consider examples shown in Fig. 2. An example in Fig. 2(a) shows two geometrical objects of a circuit layout from the same mask layer and the equivalent critical area for shortening them. Moreover, an example in Fig. 2(b) shows a geometrical object of a circuit layout and the equivalent critical area for opening it. We have proposed the following expression

$$A_{so}(x) = \frac{x-s}{8}\sqrt{x^2-s^2} + \frac{x^2}{4} \times \left(\arcsin\sqrt{\frac{x-s}{2x}} - \sqrt{\frac{x-s}{2x}}\cos\arcsin\sqrt{\frac{x-s}{2x}}\right) \tag{8}$$

for the definition of the circular part of critical area for short circuit between two geometrical objects, and the expression

$$A_{oo}(x) = \frac{x-w}{8}\sqrt{x^2-w^2} + \frac{x^2}{4} \times \left(\arcsin\sqrt{\frac{x-w}{2x}} - \sqrt{\frac{x-w}{2x}}\cos\arcsin\sqrt{\frac{x-w}{2x}}\right) \tag{9}$$

for the definition of the circular part of critical area for opening a geometrical object, where x is the defect diameter, s is the spacing between objects, w is the width of an object, and $x \geq s, w$.

Consequently, *canonical coordinates of the equivalent critical area for shortening two geometrical objects* $(x1, y1)$ and $(x2, y2)$, in the case of $s = \max(Y1_1, Y1_2) - \min(Y2_1, Y2_2)$, can be obtained by making use of the following expressions

$$x1 = \max(X1_1, X1_2) - \frac{2A_{so}(x)}{x-s} \tag{10}$$

$$x2 = \min(X2_1, X2_2) + \frac{2A_{so}(x)}{x-s} \tag{11}$$

$$y1 = \min(Y2_1, Y2_2) - (x/2 - s) \tag{12}$$

$$y2 = \max(Y1_1, Y1_2) + (x/2 - s) \tag{13}$$

but in the case of $s = \max(X1_1, X1_2) - \min(X2_1, X2_2)$ by making use of the expressions

$$x1 = \min(X2_1, X2_2) - (x/2 - s) \tag{14}$$

$$x2 = \max(X1_1, X1_2) + (x/2 - s) \tag{15}$$

$$y1 = \max(Y1_1, Y1_2) - \frac{2A_{so}(x)}{x-s} \tag{16}$$

$$y2 = \min(Y2_1, Y2_2) + \frac{2A_{so}(x)}{x-s}. \tag{17}$$

Canonical coordinates of the equivalent critical area for opening a geometrical object $(x1, y1)$ and $(x2, y2)$, in the case of $w = Y2 - Y1$, are given by the expressions

$$x1 = X1 - \frac{2A_{oo}(x)}{x-w} \tag{18}$$

$$x2 = X2 + \frac{2A_{oo}(x)}{x-w} \tag{19}$$

$$y1 = Y1 - (x/2 - w) \tag{20}$$

$$y2 = Y2 + (x/2 - w) \tag{21}$$

and in the case of $w = X2 - X1$ by the expressions

$$x1 = X1 - (x/2 - w) \tag{22}$$

$$x2 = X2 + (x/2 - w) \tag{23}$$

$$y1 = Y1 - \frac{2A_{oo}(x)}{x-w} \tag{24}$$

$$y2 = Y2 + \frac{2A_{oo}(x)}{x-w}. \tag{25}$$

The estimation of the critical area associated with lithographic defects requires averaging with respect to the defect size distribution as follows [4]

$$\bar{A} = \int_0^\infty A(x)h(x)\,dx \tag{26}$$

where $A(x)$ (A_s or A_o) is the critical area associated with defects of a given size and $h(x)$ is the defect size distribution. We use the Gamma function to describe the defect size distribution [5], [6]

$$h(x) = \frac{x^{\alpha-1}\exp(-x/\beta)}{\Gamma(\alpha)\beta^\alpha} \quad \text{for } x \geq 0. \tag{27}$$

In the expression (27), α and β are the fitting parameters which can be determined from the measured data from the following expressions

$$M(X) = \alpha\beta = \sum_{j=1}^{k} x_j f_j \tag{28}$$

$$D(X) = \alpha\beta^2 = \sum_{j=1}^{k} x_j^2 f_j - \left(\sum_{j=1}^{k} x_j f_j\right)^2 \tag{29}$$

TABLE I
YIELD MODELING RESULTS

Critical process	Wafer yield Y_i	
	CD4011B	CD4520B
1. $p^- - diffusion$	0.952	0.884
2. $p^+ - diffusion$	0.845/0.928*	0.671/0.792*
3. $n^+ - diffusion$	0.966	0.897
4. *Gate oxide* formation	0.993	0.978
5. Photoprocess *contacts*	0.984	0.949
6. Photoprocess *metal*	0.958	0.867
Final wafer yield Y	0.727/0.799*	0.428/0.505*

*after investment in $p^+ - diffusion$ process

where $M(x)$ and $D(x)$ are the mean and the variance of the measured defect size distribution, x_j is the middle of j-th interval and f_j is the normalized number of defects with the size fallen into j-th interval.

III. ANALYSIS OF YIELD LOSS MECHANISMS

By making use of the above-described yield model, yields associated with each critical process step can be determined. An example of such a characterization of integrated circuit production process is given in Table I. The data pertain rather simple CD4000 series CMOS integrated circuit production. Six critical processes (Table I) were assumed to be responsible for the yield loss, and were accompanied by in-line yield measurements and the consequent yield analysis. It can be seen from Table I that in this particular example the yield associated with p^+-diffusion was much smaller than the yields of the other process steps and, therefore, was the main cause of the wafer yield loss. It is obvious that in this example an investment in the process of p^+-diffusion would be extremely beneficial. An investment made to improve the process of p^+-diffusion (enhancement of the process cleanliness, etc.) resulted in the final wafer yield increase of over 10%. Such an yield improvement could not be achieved by any investment in any other critical process step.

The usual approach to the integrated circuit production control is based on the defect or fault density measurements, and does not take into account the dependence on the complexity of a given integrated circuit type. Therefore, the lot of wafers may be stopped regardless of the integrated circuit type. Namely, a given defect density level can enable a decent yield (and price) of simpler integrated circuit chips, but it may not be sufficient to achieve desired yield and price of more complex integrated circuit chips. The approach considered in this paper does not suffer of described disadvantage. Moreover, it can be used to forecast and characterize yields of future products in order to decide about investments which enable the desired final integrated circuit production yield.

In the considered example of production of CD4011B integrated circuits, it is estimated that the mean of the wafer yield associated with p^+-diffusion and its variance should be higher than 0.92 and lower than $3.5 \cdot 10^{-5}$, respectively, in order to ensure the acceptable value of the final wafer yield. It can be seen from Fig. 3 that the currently established p^+-diffusion process fulfills the imposed requirements. However, in the case of production of CD4520B integrated circuits, the same defect density associated with the p^+-diffusion process has resulted in the mean of the wafer yield 0.792 and its variance $2.23 \cdot 10^{-4}$, both of them being out of estimated limits presented in Fig. 3. Therefore, in order to achieve the competitive price with a possible production of more complex CD4520B integrated circuits, a further investment in p^+-diffusion process should be made.

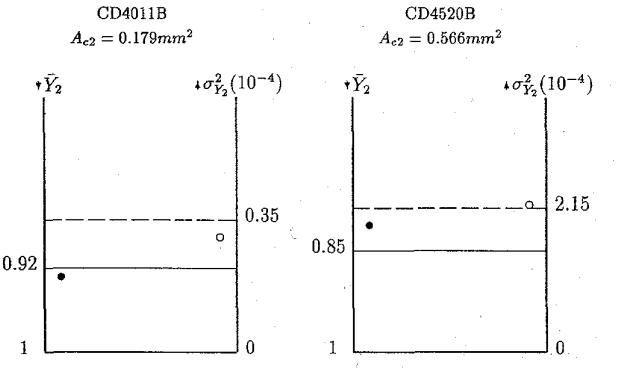

Fig. 3. The example of integrated circuit type selection ($\bar{Y}_{2\bullet} = 0.928$ and $\sigma^2_{Y_{2\circ}} = 0.29 \cdot 10^{-4}$ for CD4011B; $\bar{Y}_{2\bullet} = 0.792$ and $\sigma^2_{Y_{2\circ}} = 2.23 \cdot 10^{-4}$ for CD4520B).

IV. CONCLUSION

A yield model suited for application in a yield control system based on inline inspections of the corresponding test structures gives the opportunity for comparison of the final modeled yield and final wafer test data. When an improvement of the most critical process is carried out and a desired stability of this process is reached, we can decide about the integrated circuit types which should be produced. The usual approach to the integrated circuit production control requires estimating the defect density and does not give the opportunity for selection of integrated circuit types. However, our approach uses both yield parameters, the mean $\bar{Y}_i$ and the variance $\sigma^2_{Y_i}$ of the wafer yield distribution function, and enables sophisticated selection of integrated circuit types.

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