Development of CMOS UHF RFID Modulator and Demodulator Using DTMOST Techniques

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Abstract — *Dynamic Threshold MOSFET (DTMOST) circuits were explored for UHF RFID modulator and demodulator applications. Performance gain, power consumption, area penalty and design considerations associated with the DTMOST designs were compared and contrasted against the traditional cells. A lowered voltage supply headroom and higher speed performance using same energy per switching are observed by trading off minimum 20% more die area compared to the traditional circuits. This is due to the extra routing metals and individual well required for each DTMOST device.*

Index Terms — CMOS analog circuits, RFID, UHF integrated circuits.

I. INTRODUCTION

Application of passive Ultra High Frequency (UHF) Radio Frequency Identification (RFID) has been gaining momentum since the ratification of EPC Class 1 Generation 2 standard. Many researchers had been exploring circuit solutions to build low power high performance RFID tag. One potential technique is to use the dynamic threshold MOSFET (DTMOST). DTMOST reduces the voltage required to turn on the transistor compared to conventional transistor, due to the threshold voltage lowering effect. In the off-mode, DTMOST shares the same leakage current level as the normal transistor as both have the same threshold voltage during cut-off mode [1]. All these characteristics seemed to be good fit for UHF RFID application. This work concerns the design and analysis of both modulator and demodulator in UHF RFID tags, which are the communication modules using dynamic threshold MOSFET (DTMOST). Overview of the modulator and demodulator circuits are first presented; followed by how DTMOST devices can be substituted in conventional topologies. Design procedures and characteristics related to DTMOST-based circuits are discussed. Finally post-layout simulation results of DTMOST modulator and demodulator designed are presented, validating the design procedures proposed. The circuit simulations are implemented in standard CMOS 0.18µm triple well technology, using foundry provided BSIM3v3.24 SPICE models.

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II. MODULATOR CIRCUIT OVERVIEW

Passive UHF RFID tags do not transmit radio signals actively. Tags modulate the impedance seen by the antenna which causes some amount of incident energy to be reflected back to the reader. This type of modulated reflection is known as backscattering. To change the impedance seen by the antenna, a transistor is inserted between the two antenna terminals as shown in Fig. 1. When the transistor is turned on (conducting state), it shorts the antenna terminals, effectively presenting a short circuit that cuts off power and signal from flowing into rectifier and demodulator; when the transistor is turned off (non-conducting state), the transistor has no effect on the antenna and the rest of the modules. In this work, only Amplitude Shift Keying (ASK) scheme is investigated. DTMOST switch is investigated to form ASK modulator.

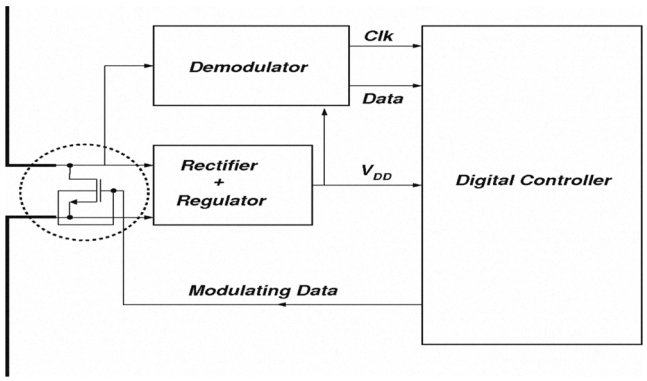

Fig. 1. Single transistor as ASK modulator

III. DEMODULATOR CIRCUIT OVERVIEW

In the RFID analogue front end, demodulator block that receives the incoming encoded RF signal converts the Amplitude Shift Keying (ASK) waveform back to baseband '1's and '0's. The proposed demodulator is shown in Fig. 2. It comprises of 2-stage voltage doublers rectifier RC low pass filter, Schmitt trigger and output inverter. The 2-stage voltage doublers will work in parallel to the power rectifier [2]. The charge accumulation capacitor (C_1) attached to the 2-stage doublers is intentionally set to have a smaller capacitance compared to the charge accumulation capacitor connected to the power rectifier. The smaller capacitance (less than 1pF) here allows the demodulator to track the dynamic range of the incoming signals, whereas the capacitor in power rectifier has very large value (several hundreds of pF) as it needs to supply steady DC current to the entire tag.

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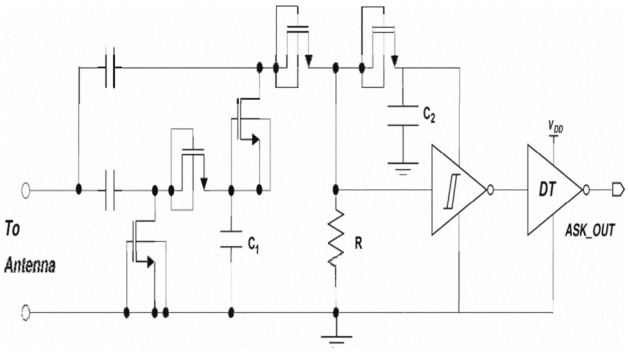

Fig. 2. Proposed demodulator structure based on DTMOST

In conjunction with this RC_1 network, the 2-stage voltage doublers effectively remove the 900MHz carrier, and leave only data. A final extra diode after the 2-stage voltage doublers is added to perform an additional rectification, removing the data signal and leaving only a slowly changing average power level. This is to provide dynamic reference for bit detection. The data signal is fed to an inverting Schmitt trigger, which is set to threshold this signal and removes associated noise and glitches. Finally an inverter is attached to act as the buffer of this data to be fed to the subsequent digital signal processing section. The last charge accumulation capacitor C_2 is chosen to have reasonable large value (tens of pF) in order to power up the inverting Schmitt trigger. This design avoids the main accumulation charge capacitor to leak its current through the demodulator resistor when the carrier is off. By isolating the resistor draining path from the main capacitor has increased the overall circuit efficiency [3].

Instead of a standard static logic inverter, a DTMOST inverter is used in the proposed demodulator. DTMOST static logic generally has higher gate capacitance than regular static logic. The higher current driving ability outweighs the increase in gate capacitance, making DTMOST gate to switch faster than regular static logic. For fixed energy/switching, DTMOST logic can be operated at higher frequency [4]. However, designers need to take in consideration that DTMOST logic has operation voltage limit, due to potential substrate diode forward biasing. In the proposed demodulator, the inverting Schmitt trigger design is shown in Fig. 3.

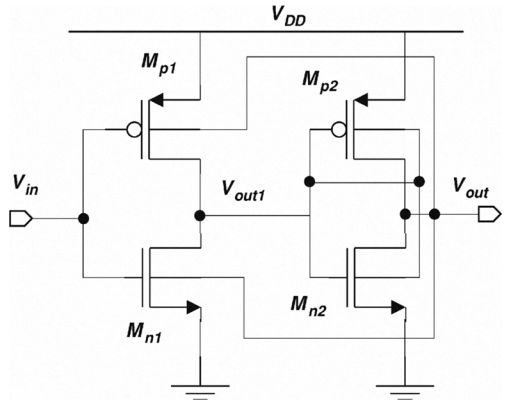

Fig. 3. Inverting Schmitt trigger based on DTMOST

This topology is first reported by [5] and it is able to work at sub-threshold V_{DD} as low as 0.4V. This circuit forbids forward body bias to exceed 0.4V. Therefore clamping diodes are not necessary. M_{p2} and M_{n2} is actually a pair of DTMOST inverter which have higher fan out capability [4]. When a low signal is applied to input port, V_{in}, V_{out} goes low. The different switching voltage or switching time causes the hysteresis. V_{out1} is buffered by the DTMOST inverter. Output is taken at the V_{out} terminal. V_{out1} has slow transition but V_{out} has a fast transition.

The switching voltage V_{hl} is given by following:

$$V_{hl} = \frac{V_{DD} - |V_{TP}| + R \times V_{TN0}}{R+1} \qquad (1)$$

Where V_{TP} is forward substrate body bias threshold voltage of PMOS, V_{TN0} is zero substrate body bias threshold voltage of NMOS, V_{DD} is supply voltage, $R=\sqrt{(k_n/k_p)}$, k_n and k_p are transconductance parameters of NMOS and PMOS respectively.

And V_{lh} is given by:

$$V_{lh} = \frac{V_{DD} + R \times V_{TN} - |V_{TP0}|}{R+1} \qquad (2)$$

Where V_{TP0} is zero substrate body bias threshold voltage of PMOS and V_{TN} is forward substrate body bias threshold voltage of NMOS.

IV. Design and Simulation Results of DTMOST Circuits

A. Design and characterization

Despite the inappropriateness of the depletion approximation when the source-substrate junction is slightly forward biased, conventional SPICE models are being used to simulate DTMOST digital gates, PISCES simulations run by [6] shows that: for short channel, the SPICE simulation using conventional model is good if substrate voltage is kept below 0.6V. Threshold voltage (V_{TH}) is important parameter Threshold voltage approximation technique is proposed to enable rapid designs of modulator and demodulator using DTMOST digital cells.

First, current-voltage (I-V) curve of DTMOST transistor of unity width over length ratio is extracted using the provided BSIM3 model. Then simple linear interpolation from the point where I-V curve deviates from the quadratic relation down to the zero current point is used to estimate effective threshold voltage of DTMOST. A graphical illustration is shown in Fig. 4. For conventional MOSFET, V_{TH} is within 0.46V ballpark whereas V_{TH} of DTMOST is around 0.36V.

After obtaining the new effective threshold voltage, equations that involve the threshold voltage parameter is updated using the new value. For example, output voltage of voltage doubler can be approximated by formula $2(V_{RF}-V_{TH}')$ where V_{RF} is the incident RF amplitude and V_{TH}' is the new

effective threshold voltage value. To obtain better results, new transconductance parameter could be obtained by curve fitting the DTMOST I-V using the usual MOSFET square law equation with the new interpolated threshold voltage value. Body effect is assumed to be negligible for simple modelling purpose.

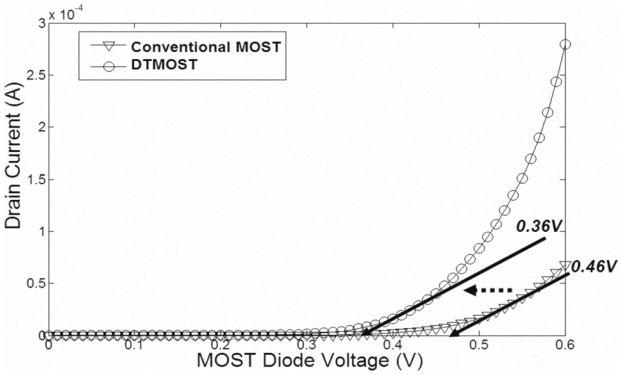

Fig. 4. Graphical approximation of DTMOST threshold voltage

After obtaining the new effective threshold voltage, equations that involve the threshold voltage parameter is updated using the new value. For example, output voltage of voltage doubler can be approximated using $2\times(V_{RF}-V_{TH}')$ where V_{RF} is the incident RF amplitude and V_{TH}' is the new effective threshold voltage value. To obtain better results, new transconductance parameter could be obtained by curve fitting the DTMOST I-V using the usual MOSFET square law equation with the new interpolated threshold voltage value. Body effect is assumed to be negligible for simple modelling purpose.

B. Post-layout simulation results

With the new set of transconductance, threshold voltage, the conventional static logic digital cells could be redesigned using DTMOST. Cells involved in the demodulator are inverter and Schmitt trigger. Layout of drawn DTMOST inverter is shown in Fig. 5. The DTMOST cell is obviously larger than conventional cell due to two factors: independent well for each MOSFET, additional length of routing metals. The DTMOST inverter increased about 20% in area size compared to conventional inverter. For more complex gate, more active area is necessary.

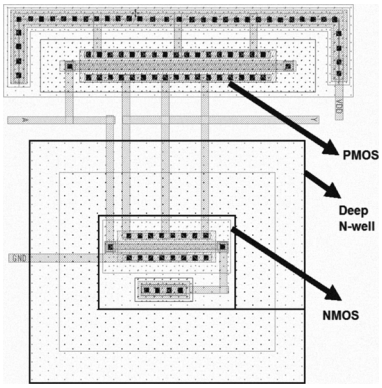

Fig. 5. Layout of DTMOST inverter

C. DTMOST Inverter simulation results

For DC analysis, the voltage transfer characteristics (VTC) of DTMOST inverters for both conventional CMOS and DTMOST logic are simulated and shown in Fig. 6. Both VTC curves are similar and approximate the ideal VTC curve, showing very good noise margin and high gain. Although such characteristics are expected in all sub-threshold logic circuits, DTMOST logic can have a higher number of fan-out, due to higher current driving capability. This allows more complex gates to be built using DTMOST without sacrificing the speed performance.

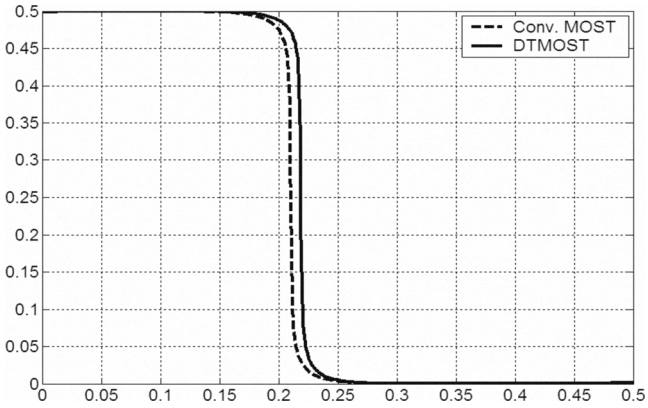

Fig. 6. VTC of conventional logic and DTMOST logic

For AC analysis, the higher current of DTMOST during active period on the negative side, causes higher power consumption; on the positive side it improves switching speed. Although generally DTMOST has higher gate capacitance, the increased current drive outweighs the effect of increased capacitance and hence still shows performance increment. Despite the big difference from the aspect of power and speed, both DTMOST inverter and conventional inverter are comparable from the perspective of power-delay-product (PDP). This implies that we can operate DTMOST inverter at much higher frequency at the expense of same energy/switching. The performance of both DTMOST inverter and conventional inverter at room temperature (25ºC) is summarized in Table I.

TABLE I
PERFORMANCE SUMMARY OF DTMOST INVERTER (DT) AND CONVENTIONAL INVERTER (CONV)

V_{DD} (V)	Delay (s)	Power (W)	Power-Delay-Product (J)
0.3	DT: 7.8×10^{-8} Conv: 7.6×10^{-7}	DT: 1.3×10^{-9} Conv: 2.0×10^{-10}	DT: 1.01×10^{-16} Conv: 1.52×10^{-16}
0.35	DT: 3.2×10^{-8} Conv: 2.5×10^{-7}	DT: 4.5×10^{-9} Conv: 7.3×10^{-10}	DT: 1.44×10^{-16} Conv: 1.83×10^{-16}
0.4	DT: 1.3×10^{-8} Conv: 1.2×10^{-7}	DT: 1.6×10^{-8} Conv: 2.4×10^{-9}	DT: 2.08×10^{-16} Conv: 2.88×10^{-6}
0.45	DT: 5.1×10^{-9} Conv: 4.5×10^{-8}	DT: 4.7×10^{-8} Conv: 7.5×10^{-9}	DT: 2.40×10^{-16} Conv: 3.38×10^{-16}
0.5	DT: 2.5×10^{-9} Conv: 1.9×10^{-8}	DT: 1.7×10^{-7} Conv: 2.2×10^{-8}	DT: 4.25×10^{-16} Conv: 4.18×10^{-16}

D. Modulator simulation results

In the simulation set up, a DTMOST is placed between the antenna terminals as in Fig. 1. A test pattern with alternating '1' (0.5V) and '0' (0V) at the speed of 100 kHz is fed to drive the gate of the DTMOST. This is to simulate the turn on and off of the DTMOST, which will short and open the antenna terminals. When the transistor is turned on, it presents a low impedance path to the incoming RF signal, lowering the effective RF amplitude seen across the antenna terminals. SPICE simulation results are shown in Fig. 7. It is found that in order to achieve similar attenuation effect, W/L of conventional transistor needs to be sized approximately 3 times larger than DTMOST.

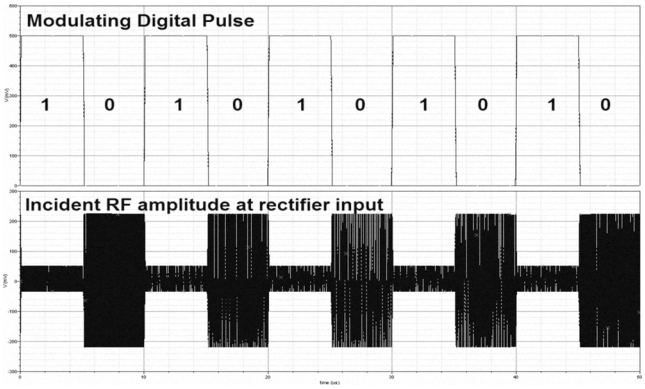

Fig. 7. Effect of modulating digital pulse on incident RF

E. Modulator simulation results

From a ASK modulated RF input signal with 500mV amplitude, the proposed demodulator is able to decode the encoded signal back to 100kHz digital baseband signal, eliminating the 900MHz carrier. The inverting Schmitt trigger is designed to have V_{lh} of 300mV and V_{hl} of 100mV. A sinusoidal signal is fed to the designed inverting Schmitt trigger. The output signal is a square wave, demonstrating hysterisis behaviour with switching threshold close to designed value. The SPICE simulations for envelope detector and Schmitt trigger are shown in Fig. 8 and Fig. 9 respectively.

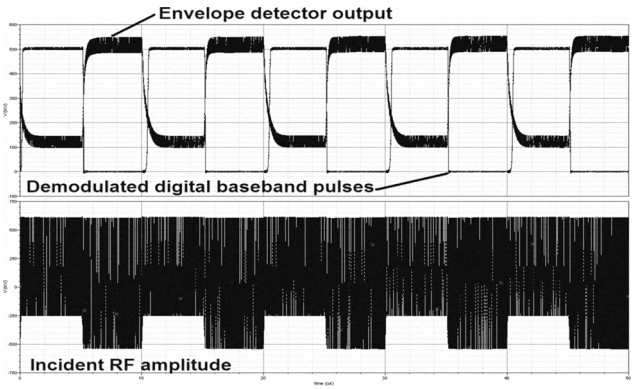

Fig. 8. Envelope detector output of demodulated signal

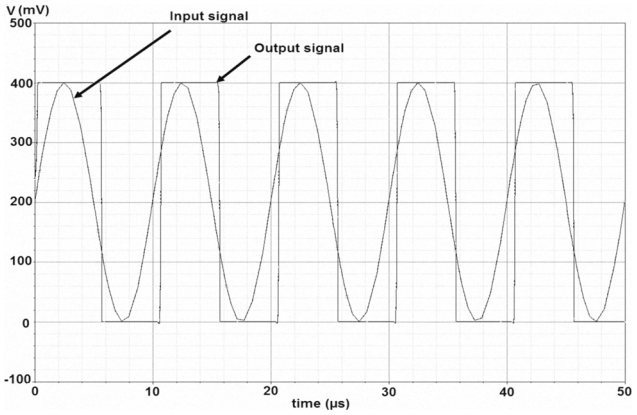

Fig. 9. Input and output of inverting Schmitt trigger

V. CONCLUSION

A simple UHF RFID modulator and demodulator structure employing DTMOST is proposed. Linear graphical threshold voltage approximation technique is applied on standard CMOS 0.18µm technology parameters. SPICE simulations validated the design technique proposed. DTMOST digital cells are able to reduce supply voltage headroom required and capable of delivering higher performance using same energy over every switching activity. The major disadvantages of the DTMOST solutions are extra 20% layout area and limited range of supply voltage due to potential forward biasing of the substrate body diode.

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