

EMC Modelling of Dual Die CPU with a Heatsink

Boyuan Zhu^{#1}, Junwei Lu^{#2}, Erping Li^{*3}

[#]*School of Engineering, Griffith University
Brisbane, QLD 4111, Australia*

¹boyuan.zhu@student.griffith.edu.au

²j.lu@griffith.edu.au

^{*}*Electromagnetics and Electronics Division*

Institute of High Performance Computing, Singapore 689048n

³eelep@nus.edu.sg

Abstract—This paper presents an EMC modelling approach for the latest dual die CPU with a heatsink from an antenna point of view. The model acts as a very efficient antenna while its structure is constructed almost according to a real dual die CPU structure. Different sizes of heatsink cooperate in the investigation of electromagnetic characterization. Simulation and measurement are accomplished in far-field range. The results show that the dual die model without heatsink is resonating at two frequencies which are 2.04GHz and 4.9GHz. When a heatsink is mounted however the resonant frequencies are changed to 1.80GHz and 5.20GHz respectively.

I. INTRODUCTION

For the purpose of achieving higher performance, various techniques are developed and implemented in the design of processors, i.e., intensive chip density, increasing clock speed and low power consumption. The result of performance evolution brings much more expectations in characterization of electromagnetic compatibility (EMC) performance as well. Therefore, different researches are investigating to predict EMC performance ahead of final fabrication for the demand of manufacturers.

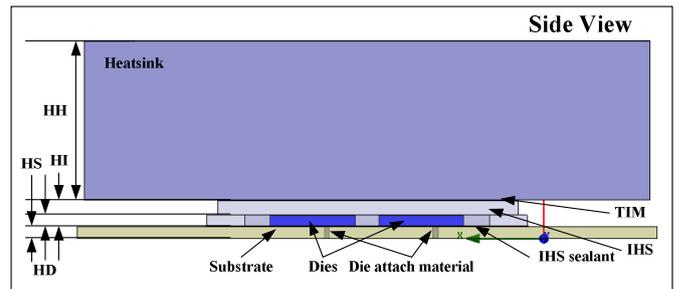
In order to provide EMC engineers and Processor vendors with a common standard which determine the validity and accuracy of their EM modeling, there is a typical model 2000-4 [1] proposed by the IEEE/EMC Society Technical Committee (TC-9) and the Applied Computational Electromagnetic Society (ACES). It is a specific electromagnetic challenging problem for the modelling of the CPU and heatsink. In this model, a traditional CPU and heatsink is modelled as a structure of a monopole antenna. As a simplified model, it ignores the package information, and the heatsink is simplified from the real structure as a solid block without fins [2]. Furthermore, some research work is extended from this model [3]-[5]

Recently, multi-die package technique has been widely used in the design of high performance processors. Taking a dual die CPU for example, two separate dies are packaged in a single package. It changes the traditional structure of internal processor and the electromagnetic performance [6] [7]. In this paper, a different modelling approach is proposed and applied on the latest dual die CPU with a heatsink. A dual die CPU is modelling with a specific patch antenna structure. Two resonant frequencies are found and verified.

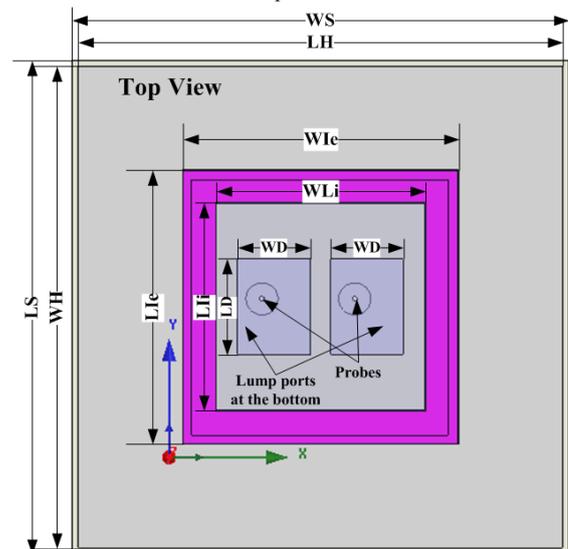
II. DUAL DIE CPU MODELLING

A. Simulation Model

The simulation model is constructed according to a real structure [8] [9], although few classified intellectual properties are instead by assumptions. According to Fig. 1 (a) and Fig. 1 (b), the constructed model consists of a substrate, integrated heat spreader (IHS), heatsink and other adhesive materials. The bottom of the substrate is grounded and two lump ports are extracted from it to give two separate internal excitations. Two probes stand through the substrate and the dies performing internal connections.



(a) Side view of model for a dual die processor



(b) Top view of model for a dual die processor

Fig. 1. Simulation model of a dual die processor with a heatsink

Modification and simplification are implemented to reduce the mesh complexity which could save simulation time and resources. From an antenna point of view, the substrate is extended to provide a more effective ground plane. When a finite ground plane is used in practice [10], the size of the ground plane should be greater than the patch dimensions by approximately six times the substrate thickness all around the periphery. This is to ensure that the results are similar to those obtained from using an infinite ground plane. As a result, a square size of 61.5 mm × 61.5 mm is applied to the ground plane in this application. Details of die size in one Intel commercial quad core chip are found in [11] with 107.0 mm² per die. Therefore, according to the practical die size, an assumption of width and length is made on the model which is 9.0 mm × 11.9 mm. The structure specification is detailed in TABLE I.

TABLE I
STRUCTURE SPECIFICATION OF INTEL DUAL DIE PROCESSOR

Name	Min	Typical	Max
Height of Heatsink (HH)		Variable	
Height of IHS (HI)		1.65 mm	
Height of Die (HD)		1.15 mm	
Height of Substrate (HS)		1.25 mm	
Depth of TIM		0.1 mm	
Depth of Die Attach Material		0.1 mm	
Depth of IHS Sealant		0.1 mm	
Length of Heatsink (LH)		Variable	
Width of Heatsink (WH)		Variable	
Length of Die (LD)		11.9 mm	
Width of Die (WD)		9.0 mm	
Length of Substrate (LS)	37.45 mm	37.5 mm	37.55 mm
Width of Substrate (WS)	37.45 mm	37.5 mm	37.55 mm
Length of IHS External (Lle)	33.9 mm	34 mm	34.1 mm
Width of IHS External (Wle)	33.9 mm	34 mm	34.1 mm
Length of IHS Internal (LLi)		26 mm	
Width of IHS Internal (WLi)		26 mm	

B. Fabrication of Test Model

A test model is manufactured according to the simulation model. A practical model is given in Fig. 2. The only difference between simulation model and test model is on the excitation ports. In test model, Two SMA connectors are installed to connect to excitation sources. In Fig. 3, it provides a structure specification of the dual die test model. The ground plane is a very thin piece of copper, melting at the bottom of the substrate. Its size is also extended. Commercial adhesive and thermal grease are used to ensure that the required parts are in complete contact with others. In addition, TABLE II lists the detailed material assignment.

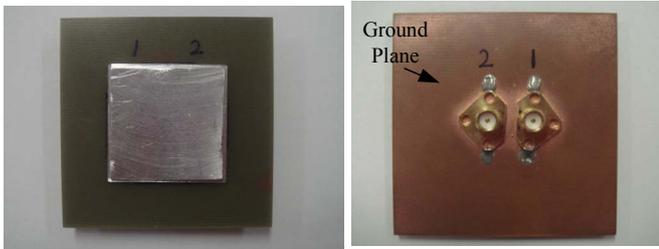
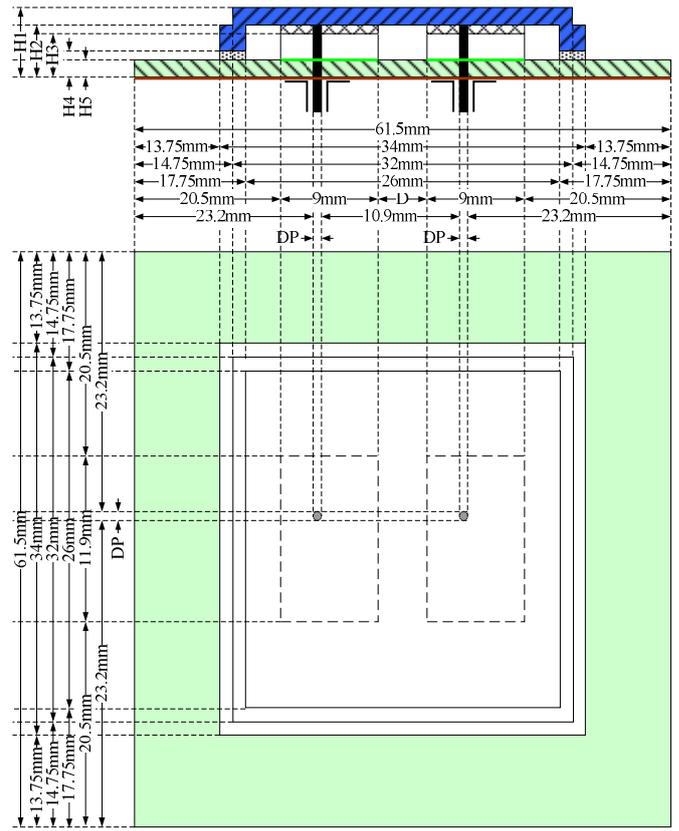


Fig. 2. Top (left) and bottom (right) view of the dual die test model



Note: H1 = 4 mm H2 = 2.5 mm
H3 = 2.4 mm H4 = 1.35 mm
H5 = 1.25 mm DP = 0.6 mm

Fig. 3. Fabrication specifics of the dual die test model

TABLE II
MATERIALS ASSIGNMENT OF FABRICATED MODEL

Name	Materials	Permittivity	Conductivity (Siemens/m)
Ground Plane	Copper	1	5.8×10^7
Substrate	FR4 epoxy	4.4	0
Die	Silicon dioxide	4	0
IHS	Aluminum	1	3.8×10^7
Probe	Copper	1	5.8×10^7
Die Attach Material	Silver, contained adhesive	1	6.1×10^7
Thermal Grease	Silver, contained adhesive	1.8	0

III. EXPERIMENTAL RESULTS

A. Reflection Coefficients

According to TABLE III and TABLE IV, comparisons between the reflection coefficient of simulation and measurement are made under corresponding configurations, at port1 and port2 respectively. For instance of port1, as shown in Fig. 4 (a), a group of simulation results at simultaneous excitations give resonant frequencies of 2.04 GHz with -18.5140 dB and 4.90 GHz with -12.01 dB while measurement results present resonant frequencies of 2.025 GHz with -16.19 dB and 4.975 GHz with -24.11 dB. Also, in

Fig. 4 (b), simulation results give resonant frequencies of 2.04 GHz with -3.783 dB and 4.80 GHz with -9.249 dB while measurement results present resonant frequencies of 2.025 GHz with -6.687 dB and 4.975 GHz with -19.48 dB at port2. According to the figures, simulation and measurement results show a good consistence at the first low resonant frequency. At the second high resonant frequency, however, the measured resonant frequencies are higher and reflection coefficients of measurement are deeper than simulation. These errors may be generated by the physical errors in fabrication and losses in measurement.

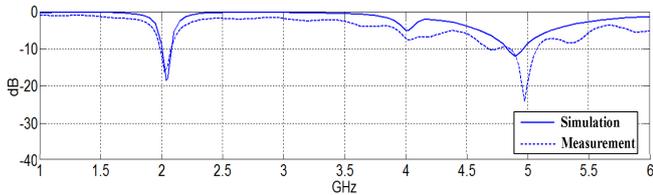


Fig. 4 (a). Reflection coefficient comparison between simulation and measurement for port1 when without heatsink

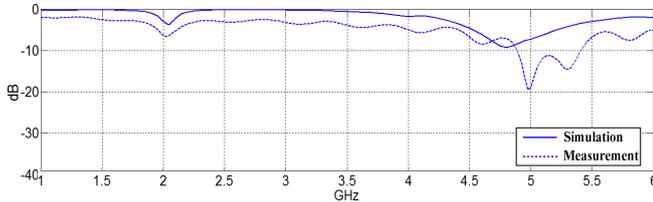


Fig. 4 (b). Reflection coefficient comparison between simulation and measurement for port2 when without heatsink

As listed in TABLE III and TABLE IV, measured resonant frequency and reflection coefficients are slightly different from the expected simulation results. In addition, modelling of a heatsink as a cubic box is simple compared to a real heatsink with fins. Also, the practical manufactory brings industry errors which make difference from the size in simulation model. Furthermore, errors and losses are introduced in calibration and measurement as well. All of these factors will introduce some acceptable errors, however they are still in a reasonably matched place.

TABLE III
REFLECTION COEFFICIENT COMPARISON BETWEEN SIMULATION AND MEASUREMENT WITH DIFFERENT CONFIGURATIONS AT PORT1

Simulation Setup	Reflection Coefficient	
	GHz	dB
Excitation at port1, open circuit at port2, no heatsink	2.07	-30.5376
Excitation at port1, 50 ohm at port2, no heatsink	N/A	N/A
Excitation at port1 and port2, with 60 mm × 60 mm × 39 mm heatsink	1.80	-12.1168
	5.50	-17.5743
Excitation at port1 and port2, with 83 mm × 64 mm × 38 mm heatsink	1.78	-9.9808
	5.39	-29.1591
Excitation at port1 and port2, with 101 mm × 76 mm × 32 mm heatsink	1.78	-10.5637
	5.38	-33.1773
Measurement Setup	Reflection Coefficient	
	GHz	dB
Excitation at port1, open circuit at port2, no heatsink	2.1625	-19.66
Excitation at port1, 50 ohm at port2, no heatsink	2.185	-25.41
Excitation at port1 and port2, with 60 mm × 60	1.775	-9.1084

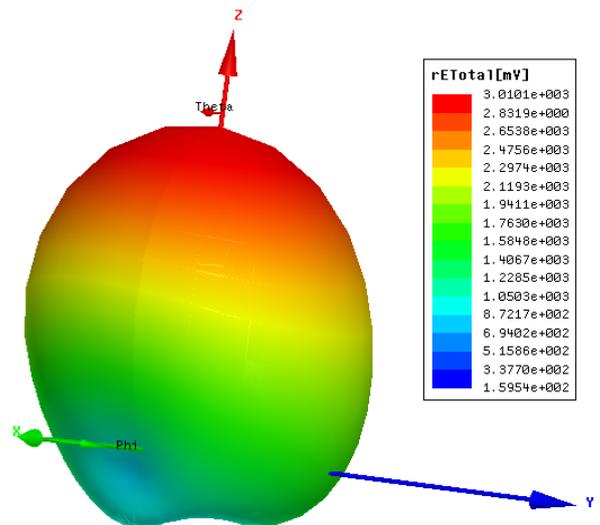
mm × 39 mm heatsink	5.525	-22.6005
Excitation at port1 and port2, with 83 mm × 64 mm × 38 mm heatsink	1.775	-9.8643
	5.275	-35.4453
Excitation at port1 and port2, with 101 mm × 76 mm × 32 mm heatsink	1.75	-8.8232
	5.25	-30.2089

TABLE IV
REFLECTION COEFFICIENT COMPARISON BETWEEN SIMULATION AND MEASUREMENT WITH DIFFERENT CONFIGURATIONS AT PORT2

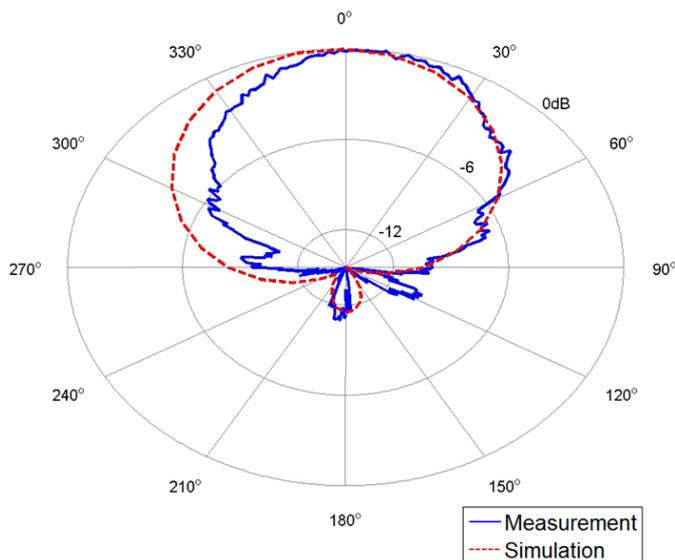
Simulation Setup	Reflection Coefficient	
	GHz	dB
Excitation at port2, open circuit at port1, no heatsink	2.14	-4.9912
Excitation at port2, 50 ohm at port1, no heatsink	N/A	N/A
Excitation at port1 and port2, with 60 mm × 60 mm × 39 mm heatsink	1.80	-3.2288
	5.19	-18.1436
Excitation at port1 and port2, with 83 mm × 64 mm × 38 mm heatsink	1.78	-2.7246
	5.15	-15.7052
Excitation at port1 and port2, with 101 mm × 76 mm × 32 mm heatsink	1.78	-2.9000
	5.15	-15.7881
Measurement Setup	Reflection Coefficient	
	GHz	dB
Excitation at port2, open circuit at port1, no heatsink	2.1175	-9.831
Excitation at port2, 50 ohm at port1, no heatsink	2.1625	-4.771
Excitation at port1 and port2, with 60 mm × 60 mm × 39 mm heatsink	1.775	-9.2974
	5.475	-27.0917
Excitation at port1 and port2, with 83 mm × 64 mm × 38 mm heatsink	1.725	-9.8853
	5.475	-27.5000
Excitation at port1 and port2, with 101 mm × 76 mm × 32 mm heatsink	1.725	-9.0000
	5.45	-32.1933

B. Far-Field

A comparison of simulation and measured far-field radiation patterns is presented for model without heatsink in Fig. 5. As presented in Fig. 5 (a), the simulation result shows radiation power emitted vertically along +Z axis. The power radiating underneath the model is very weak. With the normalised results, the radiation patterns show good agreement on both simulation and measurement for far-field in Fig. 5(b).



(a) Far-field 3-D plot of a dual die model without the heatsink



(b) Comparison of radiation pattern between simulation and measurement of the dual die model without the heatsink

Fig. 5 Far-field simulation and measurement results of the dual die model without the heatsink at 2.04 GHz

When the heatsink is mounted on the model, Fig. 6 gives a comparison of normalised simulation and measurement results in far-field. Due to losses in cables and chamber reflection, the figure doesn't match too much. The radiation direction however is the same between simulation and measurement.

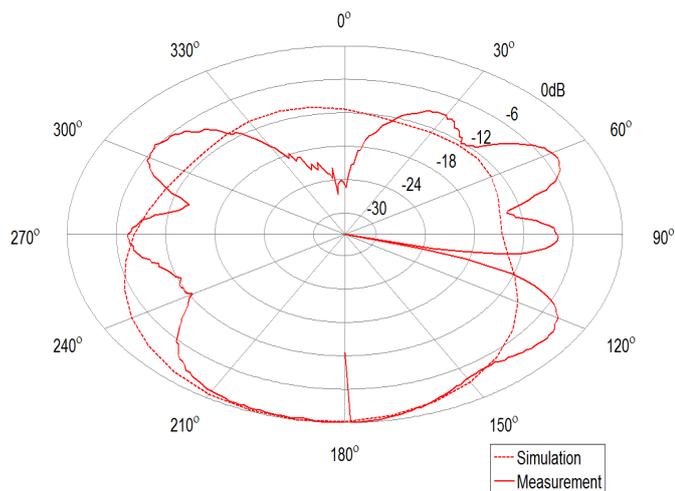


Fig. 6 Far-field simulation and measurement results of the dual die model with the heatsink at 1.80 GHz

IV. CONCLUSIONS

In this paper, a new EMC modelling approach of a dual die CPU structure with heatsink has been proposed. It provides a unique EMC prediction model in a new CPU structure and complements the former electromagnetic challenging problem 2000-4. The new model combines a real dual die CPU structure with heatsink as a microstrip patch antenna structure. Results show that the model acts as an effective antenna that generating electromagnetic interference. Reflection coefficient

measurement results show the correlation with measurement. In the range of 2 GHz to 6 GHz, the resonant frequencies of the model without the heatsink at port1 are measured at 2.025 GHz with -16.19 dB and 4.975 GHz with -24.11 dB, compared with the simulation result of 2.04 GHz with -18.5140 dB and 4.90 GHz with -12.01 dB. At port2, the measured resonant frequencies are 2.025 GHz with -6.687 dB and 4.975 GHz with -19.48 dB, and compared simulation results are 2.04 GHz with -3.783 dB and 4.80 GHz with -9.249 dB. The model of the dual die CPU with the heatsink is also verified with consistency between simulation and measurement.

ACKNOWLEDGEMENT

This work was supported in part by ARC Discovery Projects under Grant DP0772205, named "A Virtual Electromagnetic Compatibility (EMC) Lab Based on Advanced Computer Modelling and Simulation Techniques". Also, thanks to Prof. Marek Bialkowski and his Phd student Ashkan Boldaji in University of Queensland, they provided technical and equipment support for the testing model.

REFERENCES

- [1] IEEE/EMC TC-9 and ACEM website. [Online]. Available: <http://aces.ee.olemiss.edu/>.
- [2] Colin E. Brench, "Heatsink Radiation as a Function of Geometry," *IEEE Transactions on Electromagnetic Compatibility*, Aug 1994, pp. 105-109.
- [3] Junwei Lu and Xiao Duan, "EMC Computer Modelling Techniques for CPU Heatsink Simulation," *3rd International Conference, Proceedings on Computational Electromagnetics and Its Applications (ICCEA 2004)*, Nov 2004, pp. 272-275.
- [4] Junwei Lu and Francis Dawson, "EMC Computer Modelling Techniques for CPU Heatsink Simulation," *IEEE Transactions on Magnetics*, Oct 2006, pp. 3171-3173.
- [5] Junwei Lu and Xiao Duan, "Comparative Analysis of Intel Pentium 4 and IEEE/EMC TC-9/ACEM CPU Heatsinks," *IEEE International Symposium on Electromagnetic Compatibility*, July 2007, pp. 1-6.
- [6] Boyuan Zhu, Junwei Lu and Erping Li, "Electromagnetic Radiation Study of Intel Dual Die CPU with Heatsink," *The 8th International Symposium on Antennas, Propagation, and EM Theory (ISAPE2008)*, Nov 2008, pp. 1259 -1262.
- [7] Boyuan Zhu, Junwei Lu, Erping Li and Takashi Iwashita, "EMC Modelling of an Intel Dual Die CPU," *The International Symposium on Electromagnetic Compatibility*, Kyoto, July 2009, pp.521-524.
- [8] "Intel® Core™2 Extreme Quad-Core Processor QX6000 Sequence and Intel® Core™2 Quad Processor Q6000 Sequence Datasheet", Intel Corporation, Aug 2007, pp. 31-34.
- [9] Manusharow M, Hasan A, TongWa Chao and Guzy M, "Dual Die Pentium D Package Technology Development," *The 56th Proceedings of Electronic Components and Technology Conference*, June 2006, pp. 303 - 309.
- [10] Nazifa Mariam, "Design of Coaxial Fed Microstrip Antenna for LEO Satellites," *WOCN '08. 5th IFIP International Conference on Wireless and Optical Communications Networks*, May 2008, pp. 1-5.
- [11] Tom's Hardware [Online]. Available: <http://www.tomshardware.com/reviews/intel-penryn-4ghz-air-cooling,1712-5.html>.