

# Full Wave Solution for Intel CPU With a Heat Sink for EMC Investigations

Junwei Lu, Boyuan Zhu, and David Thiel

Centre of Wireless Monitoring and Applications, Griffith School of Engineering, Griffith University, Nathan, Qld, 4111, Australia

**A CPU with a heat sink (e.g. Intel Pentium 4 and Intel Pentium dual core) is a challenging problem for EMC analysis. A Very Large Scale Integrated (VLSI) device was modelled using the Finite Element Method (FEM) frequency domain solver to obtain a 3D full wave solution. The electromagnetic (EM) radiation emitted from these high power microelectronic circuits connected to a heat sink was found to have resonant frequencies around 2.4 GHz and 5 GHz with reflection coefficients less than  $-19$  dB and  $-8$  dB respectively. These resonant frequencies are very close to the operating frequency of both IEEE and Bluetooth wireless communication systems. This paper proposes a new benchmark model based on a dual core CPU and dual-source model.**

*Index Terms*—CPU, EMC, FEM, full wave solution.

## I. INTRODUCTION

**M**ODERN silicon wafer fabrication facilities easily produce transistor densities that exceed 1 million devices per die. The power generated from processor currents can exceed 100 W at high clock speeds. This combination of switching frequency and power level, in conjunction with the layout of the common mode current paths through the heat sinks, results in a significant level of radiated Electromagnetic Interference (EMI). As a result, circuit designers require an understanding of the radiated emissions from the CPU and its heat sink. Designers also need to find ways to reduce these emissions. Components such as the Intel Pentium 4, Intel Pentium dual core CPU, and AMD Athlon dual core CPU, all require separate cooling procedures provided by a fan built into their heat sink or by a fan or cooling device located adjacent to the processor.

Model 2000-4 [1] was proposed by the IEEE/EMC Society Technical Committee (TC-9) and the Applied Computational Electromagnetic Society (ACES) to provide EMC engineers and processor vendors with a common standard to determine the validity and accuracy of their EM modeling. This model is a specific and challenging electromagnetic problem for the modelling of the CPU with a heatsink. Commonly a traditional CPU and heatsink is modelled as a monopole antenna based structure. This simplified model ignores the package information, and the simplified heatsink is modelled as a solid block without fins [2]. Since these high-power and high-speed processors are common in recent computer designs, special techniques are required for EMI suppression and heat removal at the component level. In addition, 3D EM full wave based numerical analysis tools are required to model the radiated emissions. This paper focuses mainly on RF radiated emission problems that consider the CPU and heat sink as an undesirable RF radiator [3].

## II. EMC SOURCE MODELLING AND MODEL ATTRIBUTES

### A. CPU Source Model Consideration

EMC/EMI models are commonly represented as three distinct parts: the source of RF energy, the geometry of the active

and passive components, and the remaining problem space [4]. To model the CPU with a heat sink structure, it is useful to further divide the structure into three regions; the ground plane, source region and heat sink. A realistic representation of a VLSI circuit must consider the electromagnetic source characteristics and an actual physical representation such as a conducting patch [5]. Although real heat sinks have fins to increase the thermal convection loss, Brench [6] found that the heat sink could be modelled as a solid block. Das and Roy [7] modelled the source as a monopole that passes through the circuit. This EMC source model was used to address the previous problem confronting the IEEE EMC Society (486 CPU). The Intel P4 and Intel dual core CPU with a heat sink have very different structural configurations, therefore a new EMC source model is required for modelling and simulation.

### B. Intel P4 CPU Heat Sink Model

The Intel P4 processor with 478 pins has unique packaging and a different structural configuration (see Fig. 1(a)). In the Intel P4 configuration, a heat spreader is located on top of the VLSI. This heat spreader is electrically isolated from the VLSI packaging. A new EMC source model consists of a multi layered structure forming a microstrip patch antenna structure, which is resonant at frequencies of around 2.4 GHz and 5 GHz respectively [8]. This is shown in Fig. 1(b). Several clock frequencies in the band from 1.40 GHz through 2 GHz are considered for demonstration purposes, where A1 is 2.378 mm, A2 is 1.080 mm, L is 2.030 mm, L1 is 88.9 mm, W1 is 38.1 mm, W2 is 31.75 mm and W3 is 35 mm.

### C. Intel Dual Core CPU Heat Sink Model

A transverse cross-section of the Intel dual die processor with a heat sink is illustrated in Fig. 2(a) [9]. The package is a Flip-Chip Land Grid Array (FC-LGA6) and the die is located upon the substrate with the help of die attach material as shown in Fig. 2(b). The sealing is also the integrated heat spreader (IHS) covering the dies in order to protect them. Adhered by the thermal interface material (TIM), the heat sink is in full contact with the top of IHS. Like the Intel P4 CPU model, this dual core CPU model can be simplified to a dual feed microstrip patch antenna structure as presented in Fig. 3.

### D. Benchmark Model of Intel Dual Core CPU Heat Sink

Like the single source driven Intel P4 CPU [8], the location of feed points is a critical factor that affects the accuracy and validation of the simulation results. Based on the heat distribution on an existing Intel dual die CPU [9], shown in Fig. 4, the

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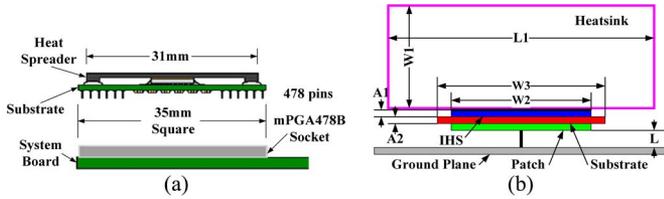


Fig. 1. Intel P4 CPU heat sink configuration and simulation model. (a) Intel P4 CPU and packaging; (b) EMC source model with a heat sink.

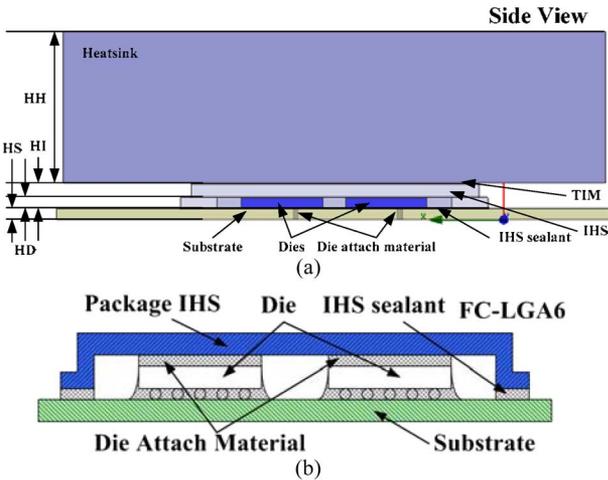


Fig. 2. Intel dual core CPU heat sink configuration and EMC source model. (a) EMC source model with a heat sink. (b) Intel dual die packaging.

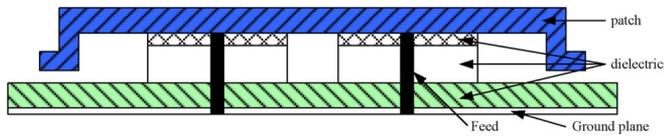


Fig. 3. Simplified dual feed microstrip patch antenna structure for Intel dual core CPU and EMC source model.

hottest point is predicted to be the area of highest current distribution where the electromagnetic interference generated is very significant. Thus the feed points of the equivalent patch were allocated to these regions for the EMC source model assuming a 50 ohm source impedance. Note that the highest current density for a driven patch antenna is immediately adjacent to these probe feeds. The size of the equivalent patch antenna model, as shown in Fig. 4 is simply the resonant size at 2.45 GHz and the second frequency at 5 GHz. However, the actual resonant frequencies may vary slightly due to the complex structure.

Modification and simplification were used to reduce the mesh complexity and to save simulation time and computational resources. From an antenna point of view, the substrate was extended in the model to provide a more effective ground plane. When a finite ground plane is used in antenna design, the size of the ground plane should be greater than the patch dimensions by approximately six times the substrate thickness all around the periphery [10]. This is to ensure that the results are similar to those obtained using an infinite ground plane. As a result, a square size of 61.5 mm  $\times$  61.5 mm was applied to the ground plane in this application. Details of die size in one Intel commercial quad core chip were taken from [9] with 107.0 mm<sup>2</sup> per die. From this true die size, the width and length of the model was

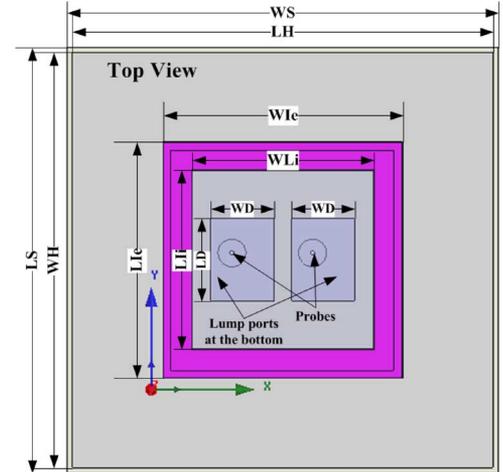


Fig. 4. Feed points of the benchmark model of Intel dual core CPU and EMC source model.

TABLE I  
STRUCTURE SPECIFICATION OF INTEL DUAL DIE PROCESSOR

Name	Min	Typical	Max
Height of Heatsink (HH)		Variable	
Height of IHS (HI)		1.65 mm	
Height of Die (HD)		1.15 mm	
Height of Substrate (HS)		1.25 mm	
Depth of TIM		0.1 mm	
Depth of Die Attach Material		0.1 mm	
Depth of IHS Sealant		0.1 mm	
Length of Heatsink (LH)		Variable	
Width of Heatsink (WH)		Variable	
Length of Die (LD)		11.9 mm	
Width of Die (WD)		9.0 mm	
Length of Substrate (LS)	37.45 mm	37.5 mm	37.55 mm
Width of Substrate (WS)	37.45 mm	37.5 mm	37.55 mm
Length of IHS External (Le)	33.9 mm	34 mm	34.1 mm
Width of IHS External (We)	33.9 mm	34 mm	34.1 mm
Length of IHS Internal (Li)		26 mm	
Width of IHS Internal (Wi)		26 mm	

determined to be 9.0 mm  $\times$  11.9 mm. The structure specification is detailed in Table I.

### III. FULL WAVE SOLUTION

#### A. Frequency Domain Modelling in EMC/EMI

The EMC modelling of a dual die CPU is a complex computation problem which requires full-wave techniques. The full-wave computational technique can provide a complete solution to Maxwell's equations within the computational domain for all conductors and materials. In this paper, frequency domain EM modelling was used. Frequency-domain codes, such as, High Frequency Structure Simulator (HFSS), solve for one frequency at a time. This is usually adequate for antenna work and for examining specific issues. Frequency-domain codes are in general faster than their equivalent time-domain codes. For example several frequency-domain simulations can usually be run in the time it would take for a single time-domain simulation. A further benefit to using frequency-domain codes is their capacity to use larger meshes for the lower frequencies, which in turn permits a shorter computation time. To cover a wide frequency

range with frequency-domain codes, a number of simulations are required.

The EMC modelling of a dual die CPU including a dual source model is a typical antenna array problem which requires a full wave solution, where the frequency domain vector wave equation for  $\mathbf{E}$  field can be written as

$$\nabla \times \frac{1}{\mu} \nabla \times \mathbf{E} + \sigma_e \omega \mathbf{E} + \omega^2 \varepsilon \mathbf{E} = -j\omega \mathbf{J} \quad (1)$$

where  $\omega$  is angular frequency,  $\mathbf{J}$  is the source current,  $\sigma_e$  is the effective conductivity, and  $\mu$  and  $\varepsilon$  are the permeability and permittivity of the problem space respectively.

A finite conductivity boundary and perfectly matched layer (PML) were applied in the simulation model. The finite conductivity boundary represents an imperfect conductor that simulates the ground plane of the CPU. The finite conductivity boundary implies an imperfect conductor where the following condition applies:

$$E_{tan} = Z_s(\hat{n} \times H_{tan}) \quad (2)$$

where,  $E_{tan}$  is the component of the E-field that is tangential to the surface.  $H_{tan}$  is the component of the H-field that is tangential to the surface.  $Z_s$  is the surface impedance of the boundary.

### B. Full Wave Solutions for CPU Heat Sink Models

Simulation results are presented in Table II, which allows a comparison between the reflection coefficient of simulation and measurement made under corresponding configurations, at port 1 and port 2 respectively. For instance of port 1 shown in Fig. 5(a), a group of simulation results at simultaneous excitations give resonant frequencies of 2.04 GHz with  $-18.51$  dB and 4.90 GHz with  $-12.01$  dB while measurement results present resonant frequencies of 2.025 GHz with  $-16.19$  dB and 4.975 GHz with  $-24.11$  dB. Also, in Fig. 5(b), the simulation gave resonant frequencies of 2.04 GHz with  $-3.78$  dB and 4.80 GHz with  $-9.25$  dB while the measurement results of resonant frequencies were 2.025 GHz with  $-6.69$  dB and 4.975 GHz with  $-19.48$  dB at port 2. From the scattering parameter  $S_{11}$  (assuming a 50 ohm source) across the frequency band, it is clear that both models have two resonant frequencies. The  $S_{11}$  results indicate that there is maximum radiation from the structure at these two frequencies. The simulation and measurement results also show a good consistency at the lower resonant frequency. At the higher resonant frequency, however, the measured resonant frequency was higher, and reflection coefficients of measurement was deeper than simulation. These errors may be generated by the physical errors in fabrication and losses in measurement as the die is electromagnetically coupled to the heat sink through the substrate.

### C. Radiation Pattern

The CPU heat sinks cause significant radiated emissions at these resonant frequencies, assuming it is possible that currents in the VLSI circuit have Fourier components at these frequencies. Figs. 6 and 7 show the comparison of far-field radiation pattern between simulation and measurement of the dual die model without the heatsink at 2.04 GHz respectively. In the simulation,

TABLE II  
REFLECTION COEFFICIENT COMPARISON BETWEEN SIMULATION AND MEASUREMENT WITH DIFFERENT CONFIGURATIONS AT PORT I AND PORT II

Simulation Setup	Reflection Coefficient at Port 1/Port 2	
	GHz	dB
Excitation at port1, open circuit at port2, no heatsink	2.07/2.14	-30.54/-4.99
Excitation at port1, 50 ohm at port2, no heatsink	N/A	N/A
Excitation at port1 and port2, with 60 mm × 60 mm × 39 mm heatsink	1.80/1.80	-12.12/-3.23
	5.50/5.19	-17.57/-18.14
Excitation at port1 and port2, with 83 mm × 64 mm × 38 mm heatsink	1.78/1.78	-9.98/-2.72
	5.39/5.18	-29.16/-15.70
Excitation at port1 and port2, with 101 mm × 76 mm × 32 mm heatsink	1.78/1.78	-10.5637/-2.90
	5.38/5.15	-33.1773/-15.78
Measurement Setup	Reflection Coefficient	
	GHz	dB
Excitation at port1, open circuit at port2, no heatsink	2.1625/2.12	-19.66/-9.83
Excitation at port1, 50 ohm at port2, no heatsink	2.185/2.16	-25.41/-4.77
Excitation at port1 and port2, with 60 mm × 60 mm × 39 mm heatsink	1.775/1.77	-9.1084/-9.29
	5.525/5.47	-22.6005/-27.09
Excitation at port1 and port2, with 83 mm × 64 mm × 38 mm heatsink	1.775/1.73	-9.8643/-9.88
	5.275/5.47	-35.4453/-27.50
Excitation at port1 and port2, with 101 mm × 76 mm × 32 mm heatsink	1.75/1.73	-8.8232/-9.00
	5.25/5.45	-30.2089/-32.19

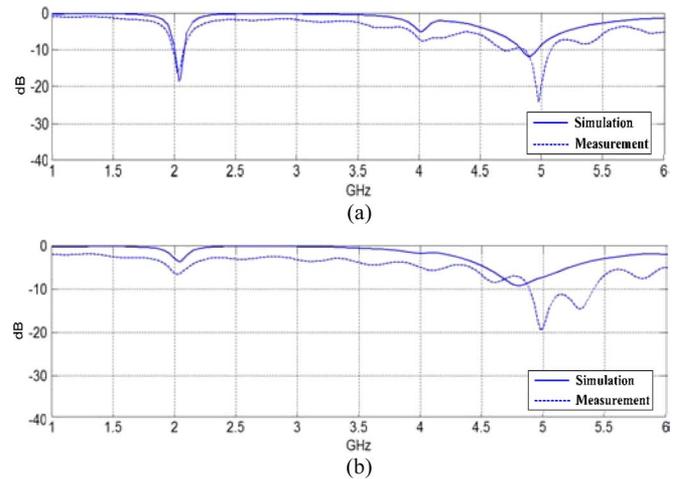


Fig. 5.  $S_{11}$  results for the Intel dual core CPU heat sink, where — line indicates the simulation results, and . . . line indicates the measurement results for both excitation cases at port 1 (a) and at port 2 (b) respectively.

the E field result was collected with a 61.5 mm × 61.5 mm rectangular plane fixed 10 mm above the model. The result is illustrated in Fig. 8. The concentration and distribution of radiation between the simulation and measurement results are almost the same, although the power of RF generator in measurement was 10 mW while the power given in the simulation is 1 W. From

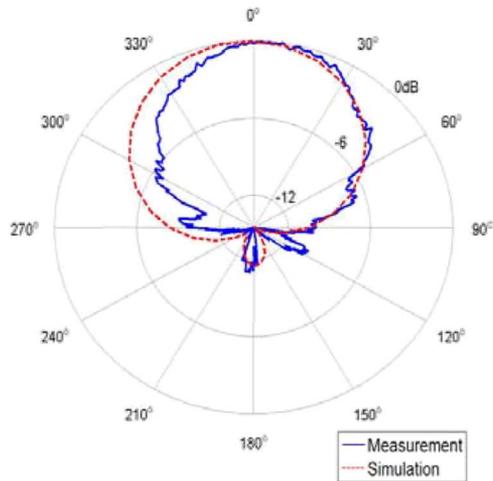


Fig. 6. Far-field simulation was calculated by commercially available frequency domain simulator, High Frequency Structure Simulator, and measurement results of the dual die model without the heatsink at 2.04 GHz.

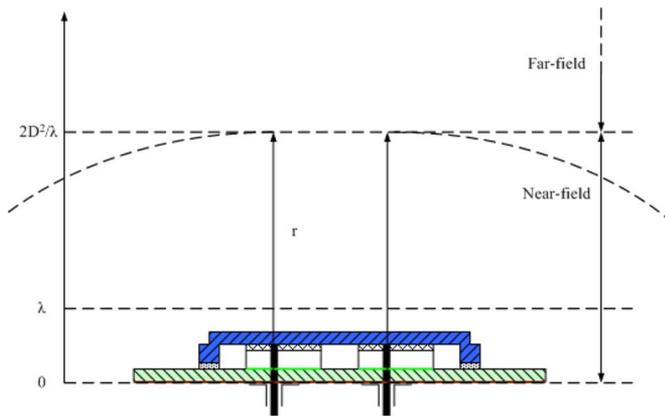


Fig. 7. Configuration of near-field simulation and measurement for the dual die model without the heatsink at 2.04 GHz.

this point, there is consistency between the simulation and measurement results.

#### IV. CONCLUSION

This paper presents a FEM frequency domain based computation technique for radiated emissions from CPU heat sink models. The CPU heat sink model is significantly different to the conventional CPU heat sink model of IEEE EMC challenge problems. The Intel P4 and Intel dual core CPU heat sink models with insulated configurations were found to radiate at 2.4 GHz and 5 GHz respectively. These two frequencies lie very close to the wireless communication range in computing systems. The source model selection for dual die CPU is critical for the CPU heat sink model as it affects the resonant frequencies associated with the CPU clock speed, the CPU core and heat sink structures. The far field and near field radiation patterns from those CPU heat sink models and validation of the CPU dual core benchmark model have been discussed.

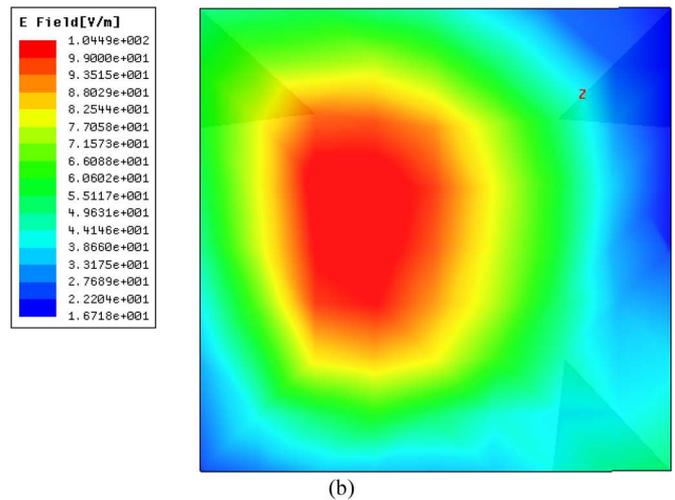
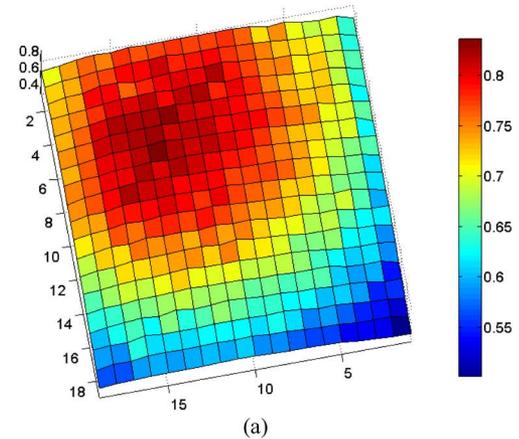


Fig. 8. Near-field measurement (a) and FEM frequency domain simulation (b) results of the dual die model without the heatsink at 2.04 GHz.

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