

# Design and Fabrication of an ECG Amplifier on Silicon Using Standard CMOS Process

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### Abstract

*The ECG is a vital part in the armory of the fight against heart disease. In this work we have designed and implemented a 6 lead ECG acquisition system on silicon. The total circuit consisting of instrumentation amplifiers and filters were placed them onto a silicon die 870 $\mu\text{m}$  by 500 $\mu\text{m}$ . The circuit shows good noise immunity, very high CMRR, and a good frequency response. The output of the circuit is a 0 to 4 volt signal for lead I and lead II. The advantage of this system is the use of the standard CMOS process which will reduce the complexity and cost of manufacture.*

### Keywords

ECG, VLSI, CMOS

ECG acquisition stage consisting of amplifiers and filters placed onto silicon, the final size of which is less than 1mm square. The advantage in the approach we have taken is that the system is created using the standard CMOS process. This will later enable both the analogue and digital parts of the circuits to be manufactured on the same die, which will reduce the size, improve the reliability, and reduce the cost of the ECG system.

This paper shows reviews the requirements for ECG measurement and details the circuit for the ECG measurement. The VLSI design for the placement of this circuit is discussed followed by the simulation results verifying the VLSI design. Finally some conclusions are drawn and both current as well as future work is discussed.

## INTRODUCTION

The electrocardiogram (ECG) is an important diagnostic tool in the detection and treatment of heart disease. The current standard in ECG measurement is through the use of bulky fixed monitoring units in a hospital ward or the use of a 'holter' monitor which is typically worn for at least 24 hours in an outpatient situation. The current push is towards telemedicine [1] which concentrates on monitoring the patient remotely. To achieve this then new technology has to be created which is smaller, more portable, more robust, easy to use, and cheap to produce. The ideal ECG system would consist of the whole ECG measurement and analysis system on a chip. We envisage a 'bandaid' type sensor which contains the sensor, amplifiers, filters, wireless communication, and inbuilt intelligence and storage. The data collected would be sent in near real time to a central repository via the internet for access by healthcare professionals [2].

In order to achieve a smaller ECG system then VLSI techniques need to be employed. This work shows the first steps towards a 'bandaid' based system with the development of the amplifiers. This front end consists of a 4 lead

## ECG MEASUREMENT

An ECG signal can vary in magnitude from patient to patient and can typically be in the range of 80-2000 $\mu\text{V}$  [3]. This will require the signal to be amplified several hundred times before it is sampled. In this case to achieve an output voltage range of 0 – 4 volts a gain of 750 is required. The small voltage of the ECG also makes it vulnerable to many types of noise. The requirements for a 6-Lead ECG acquisition device, therefore uses 3 electrodes to collect voltages from the body, since each lead is a differential measurement between the electrodes. Using Einthoven's triangle for electrode placement and lead derivation, the three leads Lead I, Lead II and Lead III can be obtained [3]. However it is not necessary to amplify all three signals as Lead II can be derived from the addition of Lead I and Lead III. The augmented leads aVR, aVL, aVF can also be found through similar calculation. Therefore the hardware is only required to produce ECG Signals for Lead I and Lead III. Since the voltages and currents from the electrodes are small in magnitude the amplifier input impedance must be very high. This requires the use of instrumentation amplifiers, due to their low impedance, good CMRR and low noise features.

The noise in an ECG signal can be larger than the actual ECG signal itself, depending on the surrounding environment. The human body is prone to Electromagnetic Interference (EMI) which is generated by electrical equipment surrounding the patient, including 50/60Hz.

Noise can also be generated from within the body. For example as muscles contract and relax they generate voltages this occurs when the patient respire or through movement, this is referred to as artifact noise.

Differential (or bipolar) amplifiers are a useful in reducing noise because of their good CMRR. They measure the difference in voltage between two differential inputs [3]. Any EMI noise that appears on the body will be expected on all electrodes (common mode signal). Therefore the differential amplifiers will remove this noise to a certain extent. EMI can also be reduced by grounding or counteracting the voltages on the body. To counteract the common mode signal a signal of opposite polarity is connected to the body thus canceling out most of the EMI noise. This is commonly known as a driven right leg and involves using an OP-Amp to invert and drive small amounts of current through an electrode to stabilize the body's voltage.

To eliminate muscle artifact simple filters can be used, for example normal muscle activity generally has a higher frequency than the ECG. Respiratory artifact can also be filtered out as it is lower in frequency (if the patient is resting) than the ECG. Ideally the patient should also be in a resting state if possible to eliminate movement artifact.

The typical digital acquisition system for ECG monitoring consists of 3 distinct parts.

1. The data collection and filtering circuitry to collect the ECG and give a clean analogue ECG signal in a useful voltage range
2. The A/D to digitize the analogue signal
3. Processing (e.g. microcontroller) to control the measurement and store/transmit the data

In this paper we are discuss step one mindful of the successive steps. ECG collection and filtering circuitry will be placed onto silicon using VLSI techniques for the standard CMOS process to achieve this.

## ECG CIRCUIT DESIGN

This section deals with the design of the amplifier and filtering stages required to measure the ECG and provide an output signal in a useful voltage range for later stages. Once the circuitry to amplify and filter the signal has been designed, it can then be transferred to silicon.

The inputs will be from three electrodes on the patient's body. The fourth electrode (RL) is a driven electrode to reduce drift (discussed later). The output was designed to be between 0V to +4V centered around +2.0V. The upper limit is 4V because the maximum supply voltage is 5V as

many amplifier components are not able to output to +5V. The design is modular allowing for easy expansion and improvements. This circuit is required to amplify the signals and to eliminate as much noise as possible. In particular, high frequency noise should be reduced before the Analogue to Digital Converter (ADC) samples it at 500Samples/s. Common Mode noise and low frequency noise should also be minimized.

Figure 1 shows a block diagram for one lead and associated driven right leg circuit. Another lead is easily added through duplication of this circuit (excluding the driven right leg). As can be seen the circuit naturally breaks into 3 distinct stages

- |         |                             |
|---------|-----------------------------|
| Stage 1 | Amplification and Feedback  |
| Stage 2 | Filtering                   |
| Stage 3 | Amplification and DC Offset |

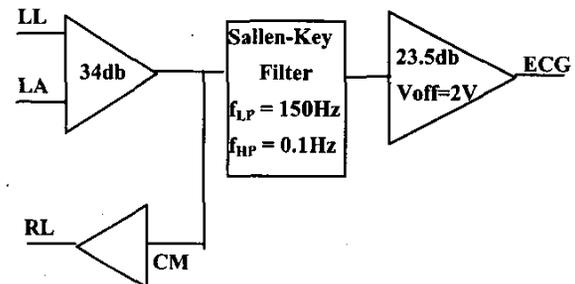


Figure 1. Block Diagram of the one lead and driven right leg ECG Circuit

The first amplification stage is one of the most important stages. The amplifiers have to be able to produce a high gain and have to have a good common mode rejection ratio (CMRR). The amplifiers must also have high input impedance and produce minimal noise. Instrumentation amplifiers were chosen for this stage as they have the ability to produce large gain and exhibit good CMRR characteristics. The CMRR is important because the input signal often have high noise components.

The common mode signal is inverted in the right leg drive and is connected to the patient's right leg. This provides unity gain negative feedback to the circuit, opposite to the noise from the patient's body. This helps to cancel out any noise that is common on the input electrodes. Care must be taken not to exceed the relevant standard for Patient auxiliary current limit, which is 0.01mA DC and 0.1mA [4]. The shield drive circuit is an Opamp, which inverts and amplifies the common mode signal, a 500k resistor is used to limit current into the body.

The filtering stage uses a second order unity-gain Sallen-Key highpass and lowpass filter to remove unwanted noise and any DC offset voltages. These filters were chosen because of their small component requirements and simple

design. The filter for the input stage is not essential to operation of the input stage and so a higher order filter was not chosen. The purpose of the filter is to remove any high frequency noise that could cause aliasing errors to occur in the subsequent sampling stages. The highpass filter reduces the drifting potential of the body and has a cutoff frequency of approximately 0.1Hz which required  $R=34K$  and  $C=47nF$ . The lowpass filter has a cutoff frequency of approximately 150Hz which required  $R=68K$  and  $C=15nF$ .

A second amplification stage is required to amplify the signal after it has been normalized to GND. This is necessary because the electrodes have a contact resistance, this highly variable resistance causes small DC voltage offsets in the input signals. If this were to be amplified the total 500 times in one stage, the signal would most likely clip or remain at  $V_{cc}$  or  $V_{ee}$ . The amplification and DC offset is achieved simultaneously using an Opamp, which has its inverting input biased so that it will produce +2V output with an input of 0V on the non-inverting input. The bias for this is generated from a resistor voltage divider buffered through an OP-Amp.

## VLSI DESIGN

The VLSI design required taking the discrete circuit described in the previous section and converting it for placement on silicon with the area of silicon being paramount in mind. The circuit was also designed so that it could be fabricated using standard CMOS process to allow manufacture by the MOSIS foundry [5]. The design process required a small reworking of the circuit since the basic structure remained the same and subsequent testing and fine-tuning of the circuit through simulation. The tools used for the VLSI step were the MENTOR suite [6].

The basic building block used throughout the design was the Opamp. The Opamp design used here is a standard differential input single ended transconductance amplifier. The Opamp consisted of a differential input stage with gain stage, a second gain stage including compensation, and an output stage. The layout of the Opamp employs overlapping transistors, which reduce the overall area of the circuit. This also helps to reduce parasitic resistances and capacitances.

Although this Opamp can be used throughout the circuit it is not suitable for use in stage 1 amplification which requires instrumentation amplifiers. This is due to requirement of a gain of 50 in the first stage and a gain of 15 in the last stage. Therefore this required the construction of instrumentation amplifiers based around this Opamp. The instrumentation amplifier was created using two of the Opamps in a differential circuit giving a fixed differential gain, a high input impedance, a high CMRR and good noise immunity. The implication of this is that a greater circuit area was required due to the use of two Opamps.

The basic structure of the whole circuit was maintained; however, some changes were made in order to condition the signal and obtain components with small values enough to fit into the IC. The most important change is in the low pass filter. The 150Hz cut off frequency of the filter makes the selection of the passive components too large to be fabricated in silicon. For instance the resistance for the filter is  $68k\Omega$ , practical for implementation, but the capacitor is 15nF, that is non practical value for silicon realization. The strategy followed to solve the problem, was to adopt the typical methodology for analog CMOS filters construction. That is using switching capacitors (SC) filters. This kind of architecture use switches, implemented with NMOS transistors, combined with capacitors to make elements that behave as resistors and allows the desired small values. However SC filters bring some implications such as voltage level of the signal and at the same time could introduce switching noise. That is the reason why the gain of the stages was changed. The total gain remains the same, but the individual gains were decreased or increased to fit the signal conditioning to the filter stage.

The cutoff frequency for the lowpass is dependant upon the ratio of two capacitors ( $C/C_r$ ). The capacitors were chosen to satisfy two requirements. The first one is that the capacitors should be large enough, so the parasitic capacitance of the switching transistors is small in comparison and the switching noise is minimized. The second one is that the capacitors must be small enough to minimize chip area. After some simulations the best result that satisfies these two requirements is with  $C = 20pF$  and  $C_r = 1.26 pF$ . In order to suppress switching noise a non overlapping phase clock is used. The layout for the SC block is the biggest in area, although is the one with less components due to the area of the capacitors compared which is very much larger than the NMOS transistors

The final gain and offset stage were straight forward to convert. The most important factor to take into account was the resistor values. If the resistor values are too small the Opamp cannot generate the necessary current but if the resistor values are too high then too much area is consumed. It was found that a resistance of  $100K\Omega$  satisfied both criteria.

Figure 2 shows the final layout of the circuit. The physical dimension of the layout are  $870\mu m$  by  $500\mu m$ . It is obvious from the layout that the capacitances take the largest area. The duplication of the circuit for each electrode can be clearly seen. This is so that the 3 input electrodes can be used to generate the differential lead signals for lead I and III.

The final layout has been prepared and is awaiting fabrication at the time of press.

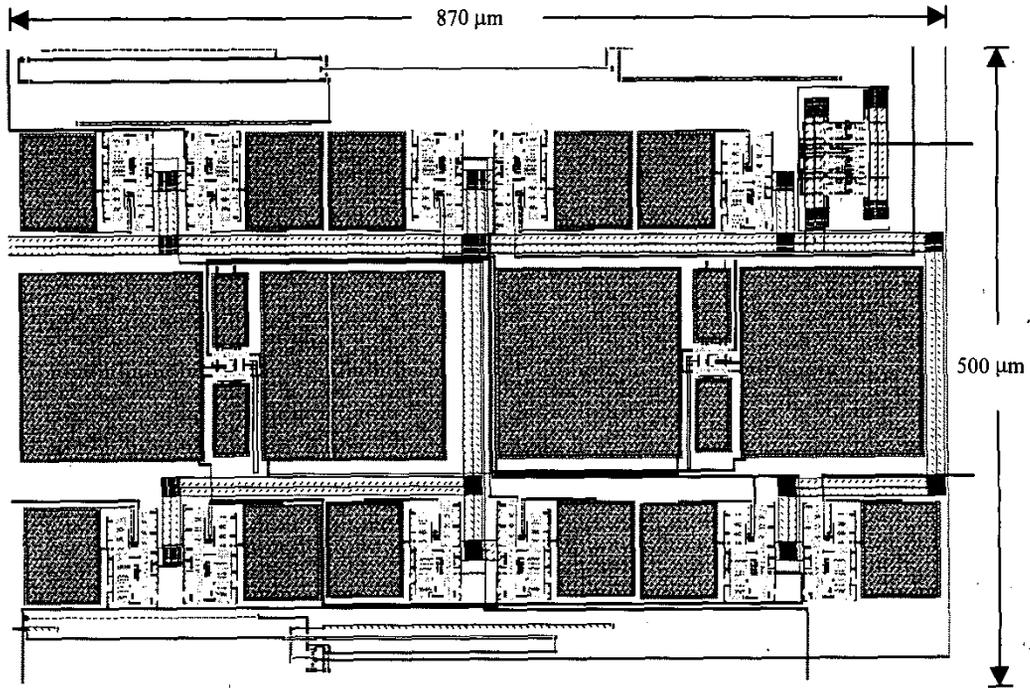


Figure 2. Final layout of the ECG circuit for manufacture

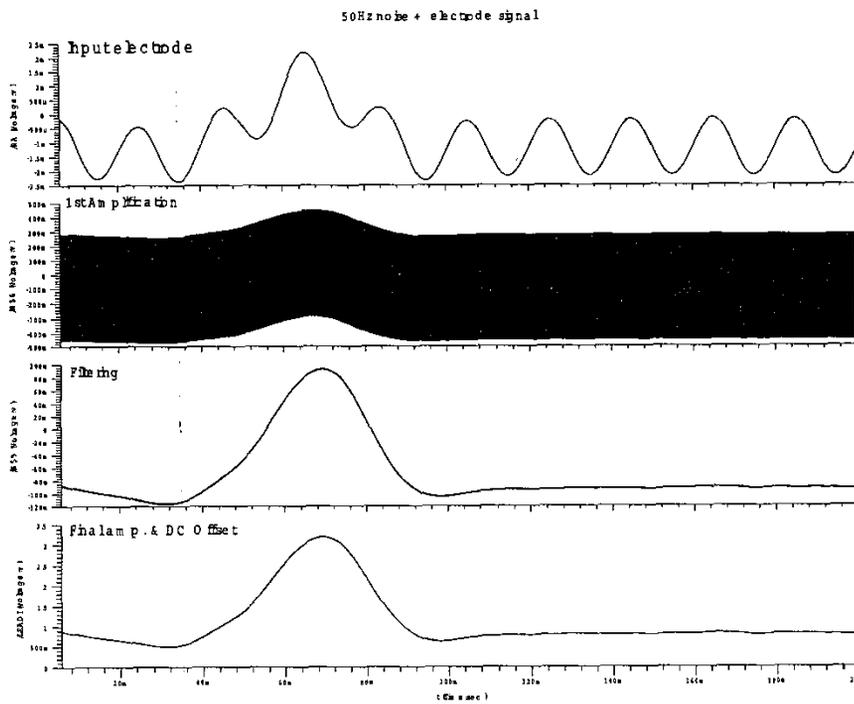


Figure 3 Signal path for an ECG like signal through the different stages of the circuit

## TEST RESULTS

As mentioned in the previous section this circuit has been sent to the foundry for manufacture. Therefore the results presented are the simulation results, demonstrating the operation of the circuit.

Figure 3 shows the results of the simulation for the 3 stages of the circuit and their response to an ECG like input signal which is given in the first panel. The second panel shows the response of the first amplifier. The filled in appearance of the figure shows the extraction point for this signal is where it is mixed with the 15KHz chopping signal for the switched capacitor filter. The third panel shows the results of the filtering. As can be seen the noise has been removed. The last panel shows the final signal amplified and offset as expected.

## CONCLUSION AND FURTHER WORK

This paper has detailed the design of a 6 lead ECG acquisition system on silicon using the standard CMOS process, for fabrication by the MOSIS foundry. The design has determined that the ECG the circuit required a gain of 750, should have very high input impedance, have a good frequency response, have good immunity from noise, and produce an ECG output voltage such that it can be easily read by an external ADC ( 0 – 4 Volts centered around 2V). The circuit design was then converted using VLSI techniques to a layout for fabrication using a standard CMOS process. The basic structure of the circuit remained the same except for the filter circuit. In order to reduce the size of the capacitor on the die a switched capacitor circuit was used.

The layout was simulated using the Mentor Graphics tools and the correct operation of the VLSI circuit was verified by injecting appropriate signals. The final size of the layout was 870 $\mu$ m by 500 $\mu$ m. This design is currently at the foundry.

At the moment we are extending this work to make an 8 channel version of the circuit with programmable amplifier gain and filter stages. Currently this work is being extended upon so that the acquisition circuitry, the ADC, and the microcontroller will appear on the same die.

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